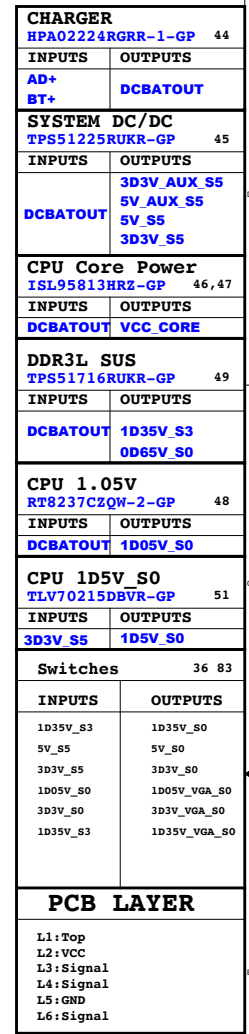



Cedar/Janus Block Diagram



PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Signal

<Core Design>		
 <div style="display: inline-block; vertical-align: middle; margin-left: 20px;"> Wistron Corporation 21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div>		
Title		
Block Diagram		
Size	Document Number	Rev
C	Janus HSW 40/50/70	X02
Date:	Friday, February 07, 2014	Sheet 2 of 104

(Blanking)

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<Core Design>



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Title

(Reserved)

Size
A4

Document Number

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Rev
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SSID = CPU

Layout Note:

Impedance control: 50 ohm

[24,42,44,46] H_PROCHOT# <<<>>>

[36] H_THERMTRIP_EN <<<>>>

Layout Note: Close to CPU

[12] DDR_PG_CTRL <<<>>>

Layout Note:

Design Guideline:

SM_RCOMP keep routing length less than 500 mils.

71.HASWE.G0U

Layout Note:

Place close to DIMM

<Core Design>



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Title

CPU (THERMAL/MISC/PM)

Size
A4

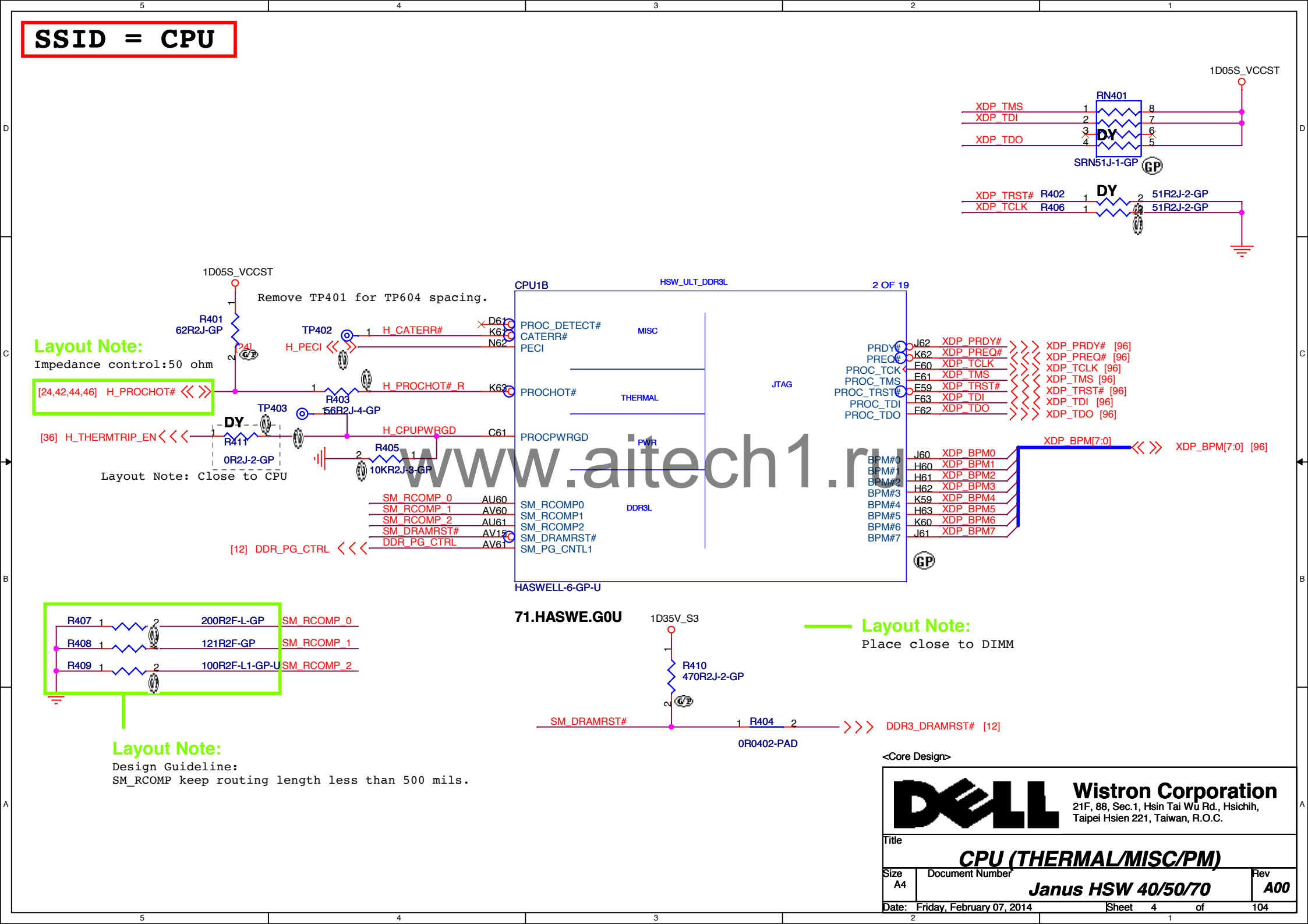
Document Number

Janus HSW 40/50/70

Rev
A00

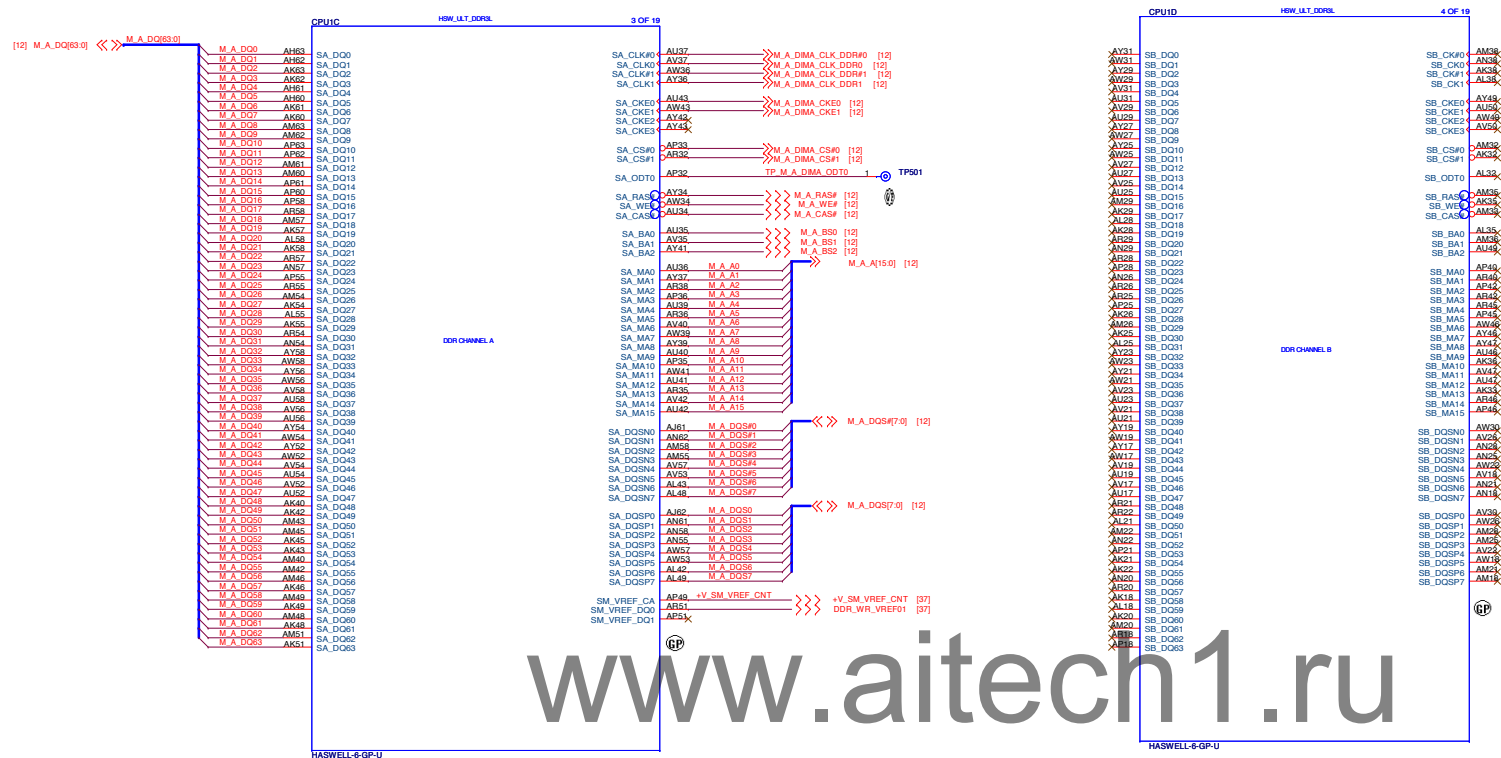
Date: Friday, February 07, 2014

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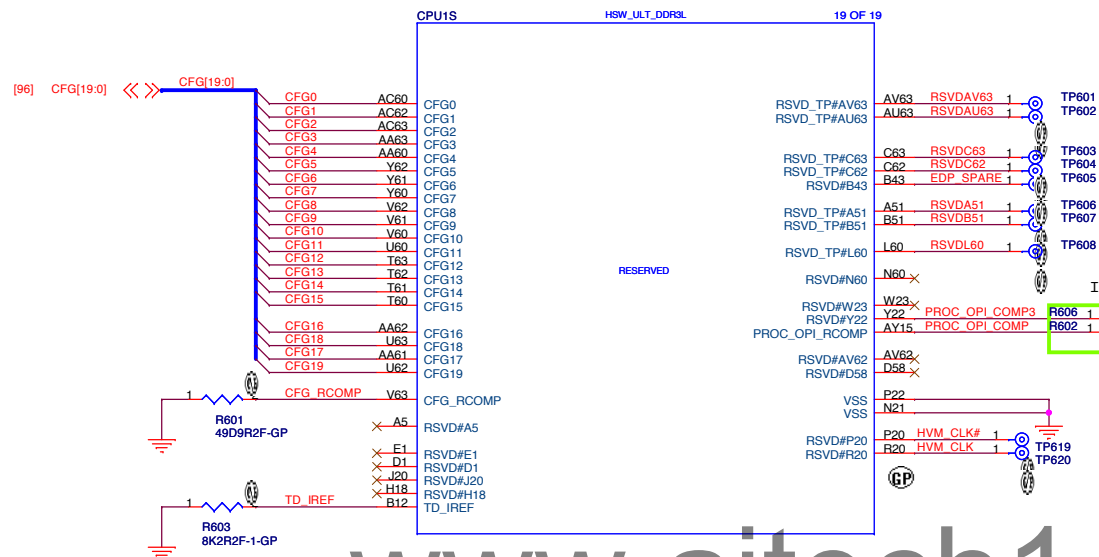
SSID = CPU

DDR3L ball type: Non-Interleaved Type



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SSID = CPU



#514405

7.4

Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD_TP - these signals should be routed to a test point
- RSVD_NCTF - these signals are non-critical to function and may be left unconnected

Intel Recommend

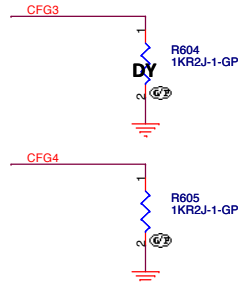
Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

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#514405 PCH strap pin:

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none">• CFG[2:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.• CFG[3]: MSR Privacy Bit Feature<ul style="list-style-type: none">— 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting— 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden• CFG[4]: eDP enable<ul style="list-style-type: none">— 1 = Disabled— 0 = Enabled• CFG[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lanes.	I/O GTL



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

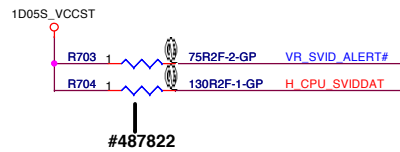
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

<Core Design>

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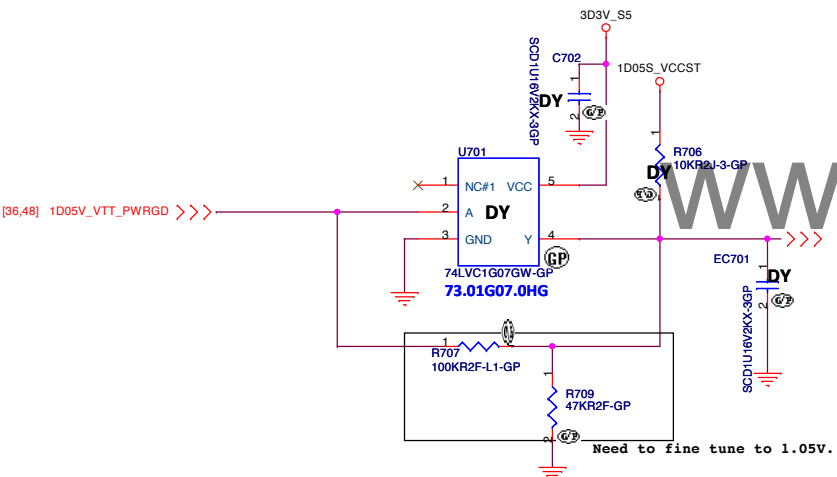
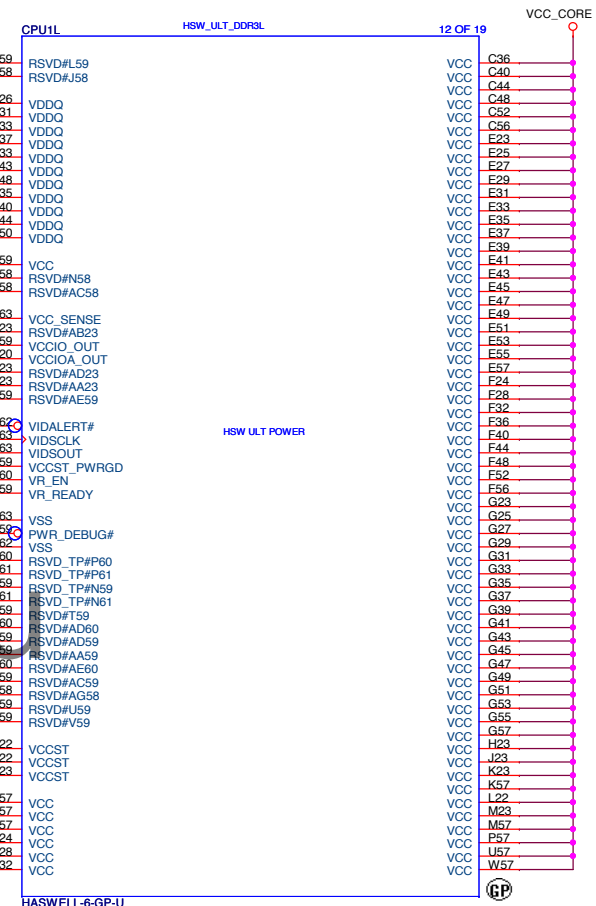
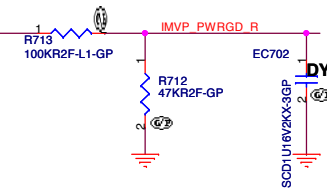
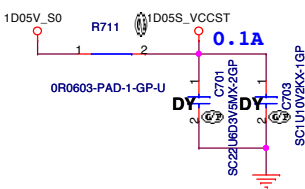
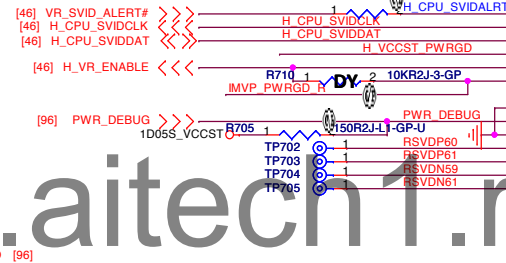
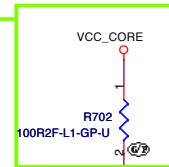
Title			CPU (CFG)
Size	Document Number	Rev	A00
A3	Janus HSW 40/50/70		
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SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

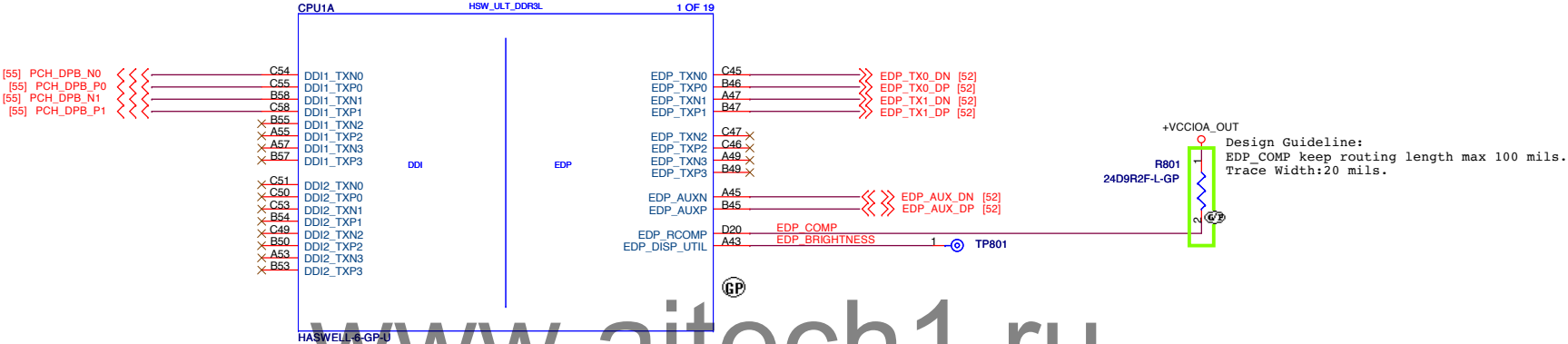


Need to fine tune to 1.05V.

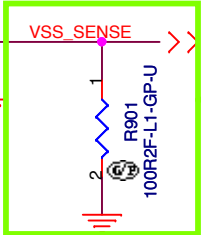
SSID = CPU

www.vinafix.vn

DP to VGA Converter



SSID = CPU



- **Layout Note:**

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

<Core Design>



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Title

CPU (VSS)

Size
A4

Document Number

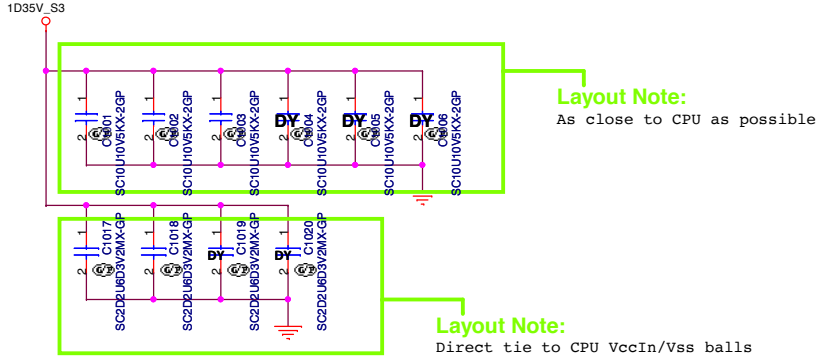
Janus HSW 40/50/70

Rev
A00

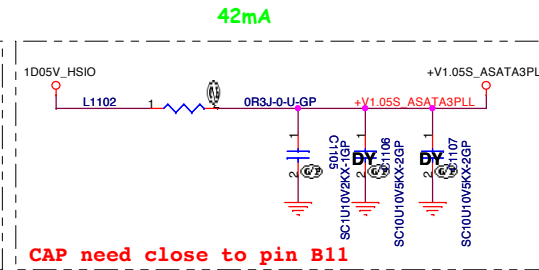
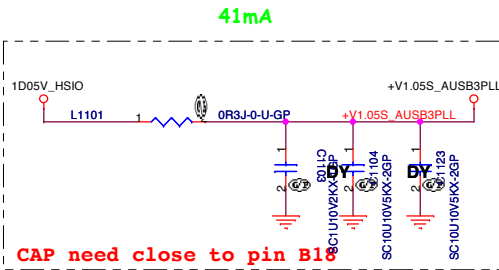
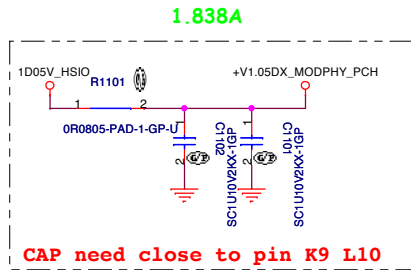
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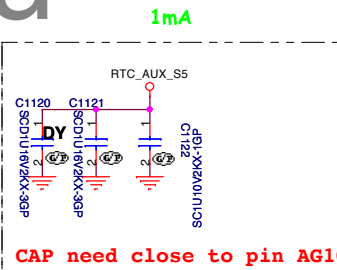
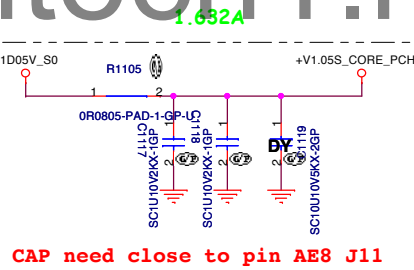
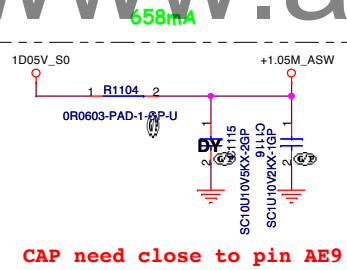
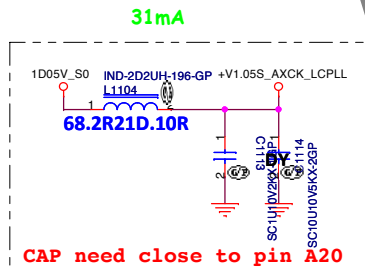
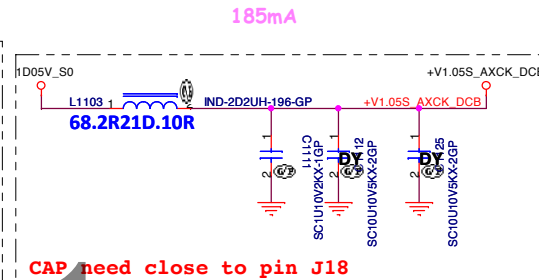
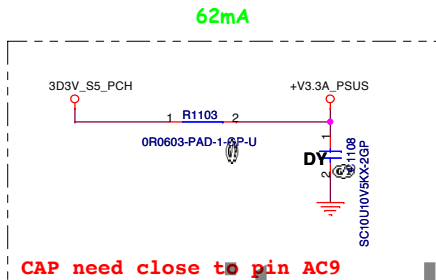
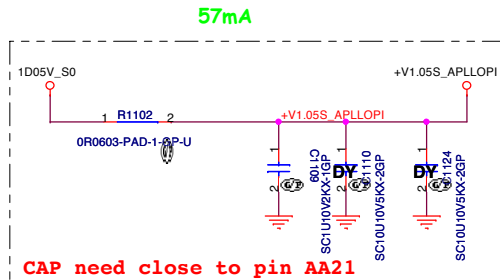
SSID = CPU



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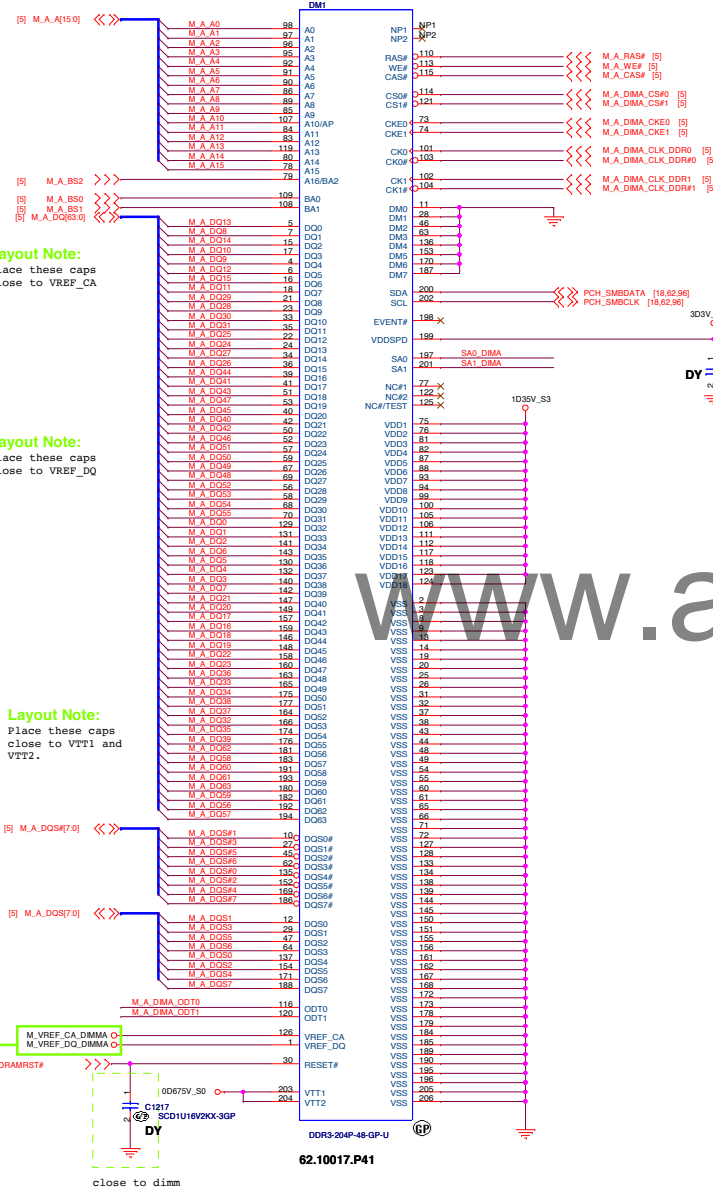
MAX: 1.92A



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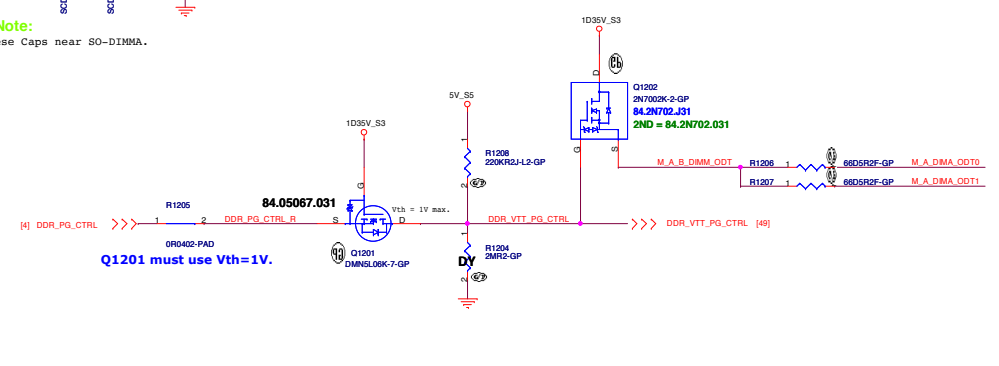
SSID = MEMORY



Note:
SA0 DIM0 = 0, SA1 DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

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Layout Note:
Place these Caps near SO-DIMMA.



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Title
(Reserved)DDR3-SODIMM2

Size
A3

Document Number
Janus HSW 40/50/70

Rev
A00


Date: Friday, February 07, 2014

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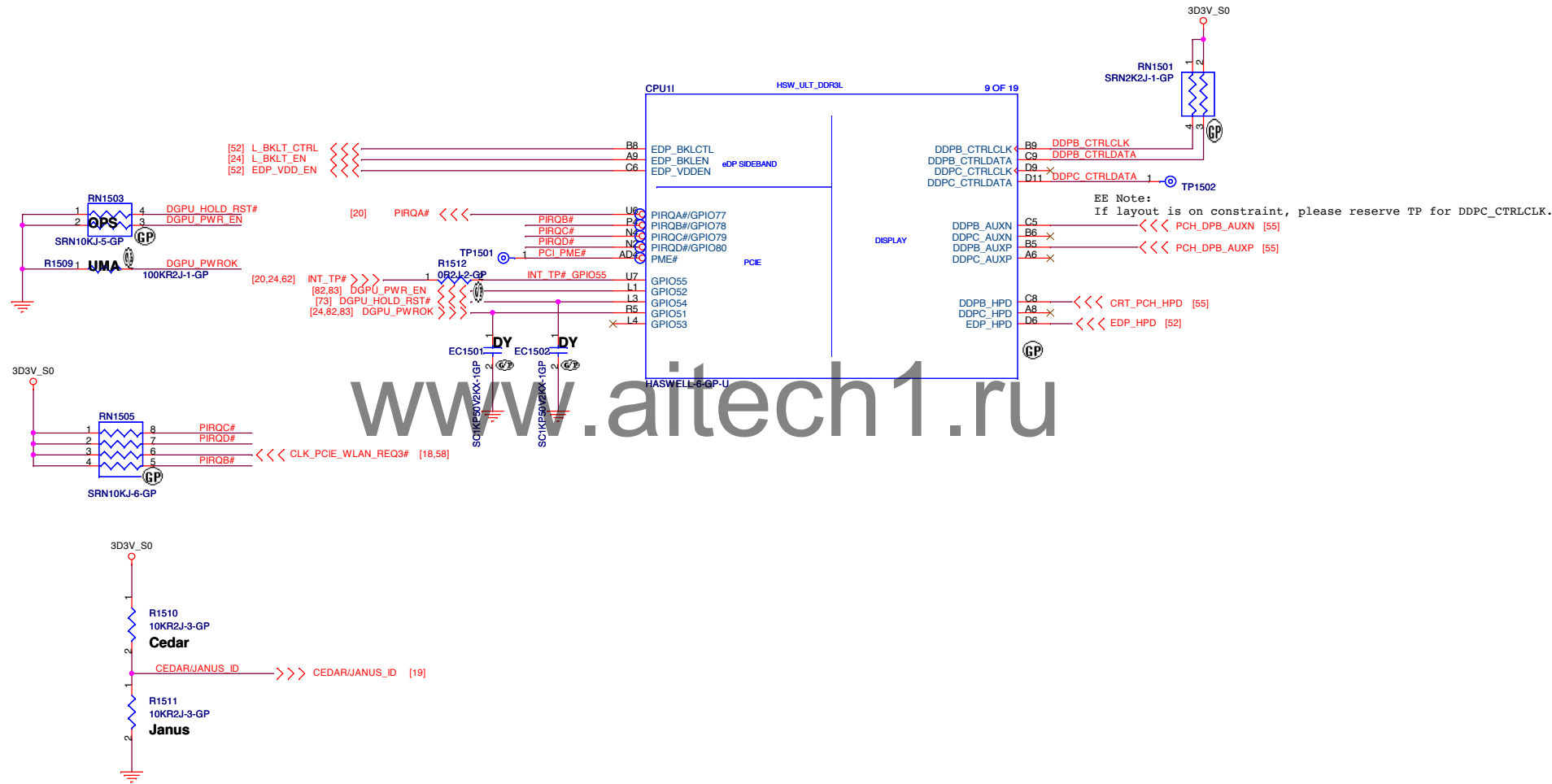
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)_SODIMM _SODIMM4		
Size A4	Document Number Janus HSW 40/50/70	Rev A00
Date: Friday, February 07, 2014		Sheet 14 of 104

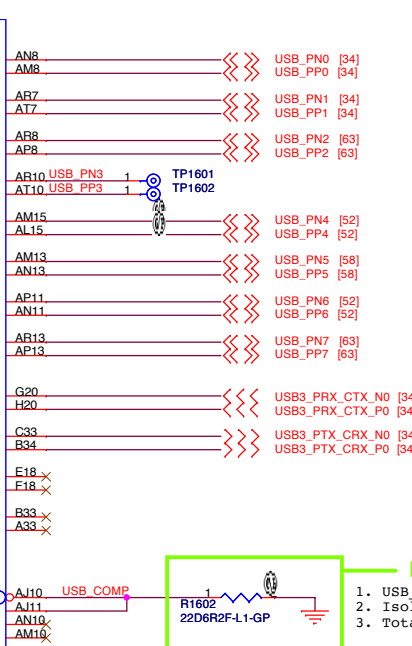
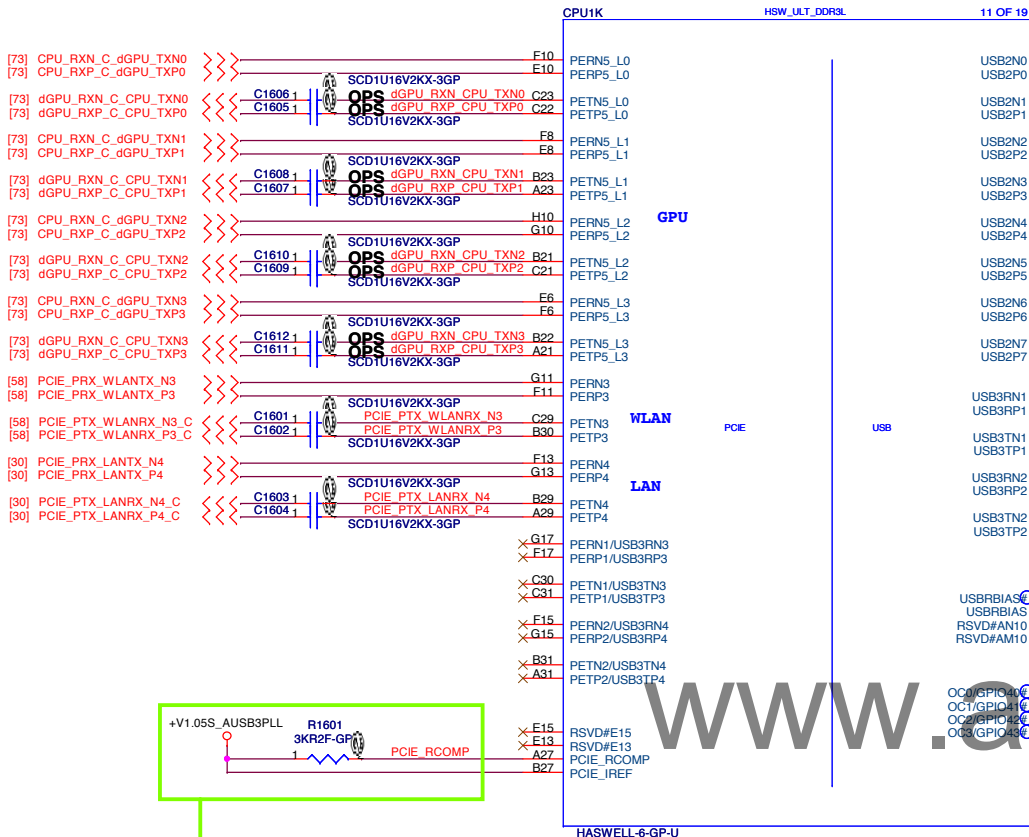
PCH strap pin:

Port B Detected	
DDPB_CTRLDATA	<div> <div></div> <div>Low = Disable Port B (default) High = Enable Port B</div> </div>
DDPC_CTRLDATA	<div> <div></div> <div>Low = Disable Port C (default) High = Enable Port C</div> </div>

The internal pull-down is disabled after PLTRST# deasserts.

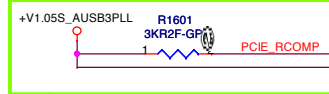


SSID = PCH



Layout Note:

1. USB COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil



Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12-15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5 (L0-L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	ODD	SATA1
6 (L0-L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

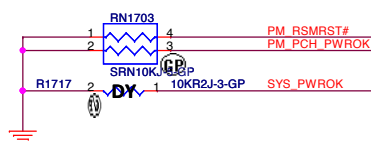
SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD		

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Title: **PCH (PCIE/USB)**
Size A3 Document Number: **Janus HSW 40/50/70** Rev **A00**
Date: Friday, February 07, 2014 Sheet 16 of 104

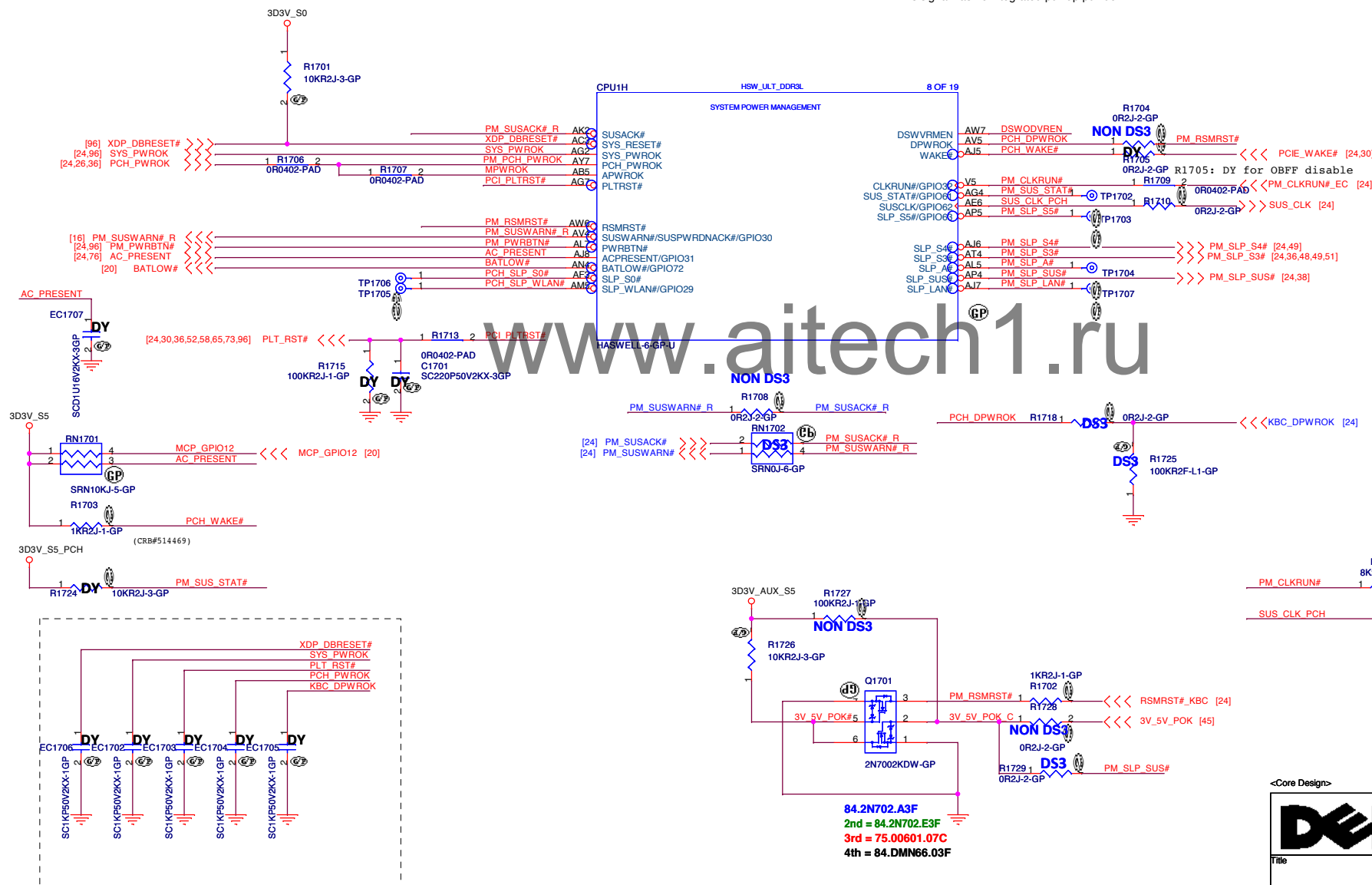
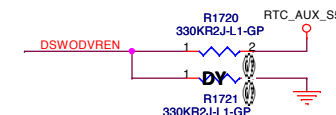
SSID = PCH



PCH strap pin:

On Die DSW VR Enable	
DSWVRMEN	Low = Disable * High = Enable (default)

This signal has no integrated pull-up/pull-down.



<Core Design>

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PCH (PM)

Size
A3

Document Number	
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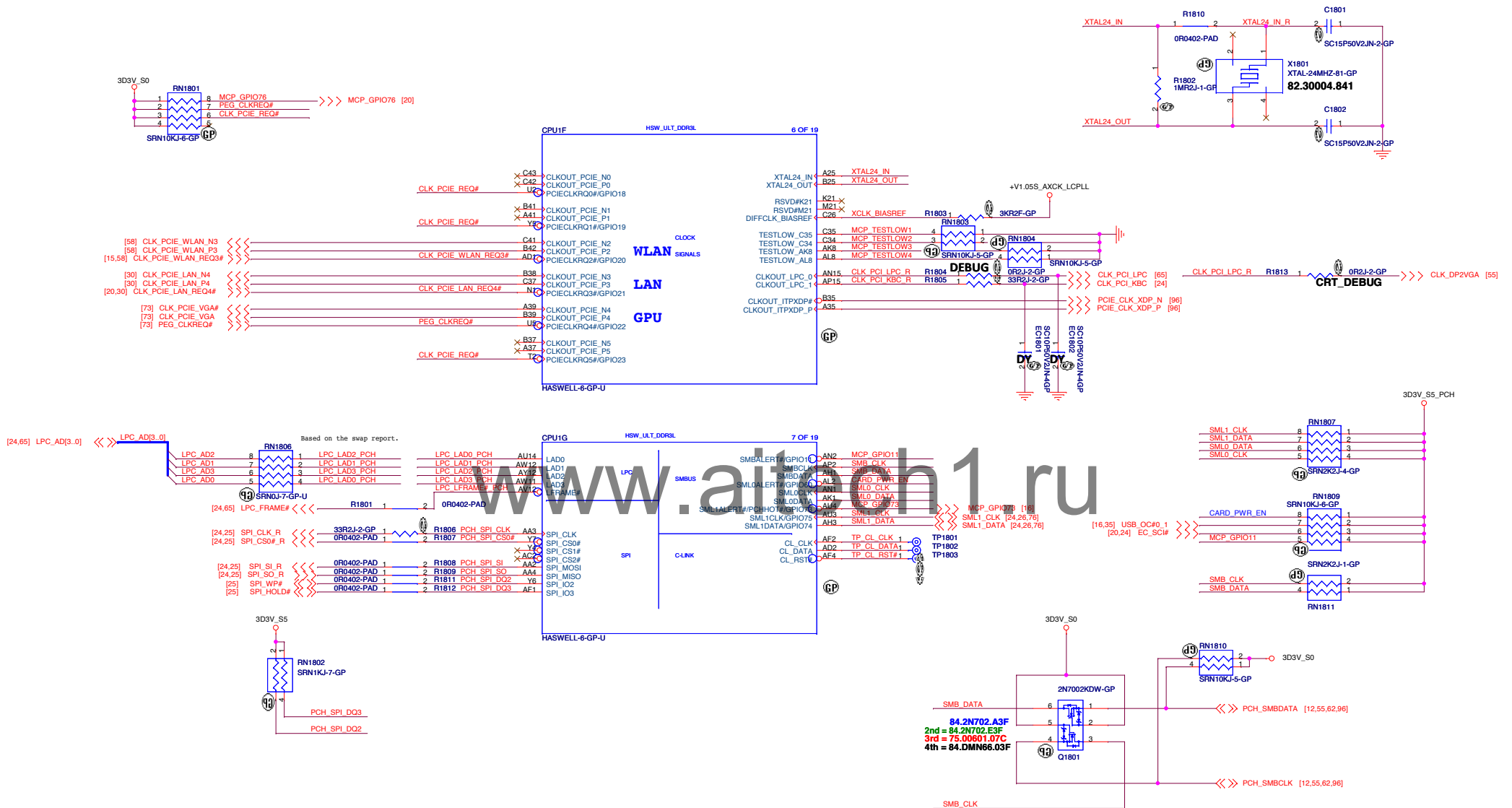
Janus HSW 40/50/70

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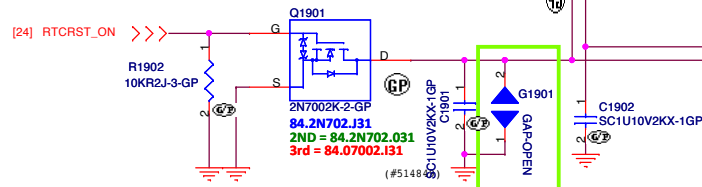
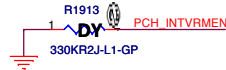
SSID = PCH



SSID = CPU

PCH strap pin:

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

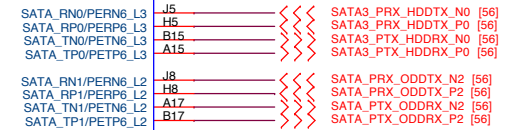
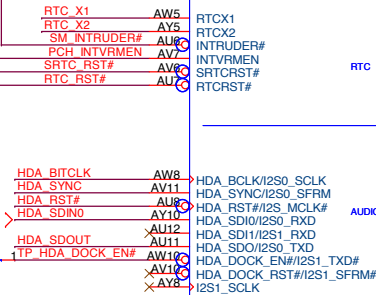
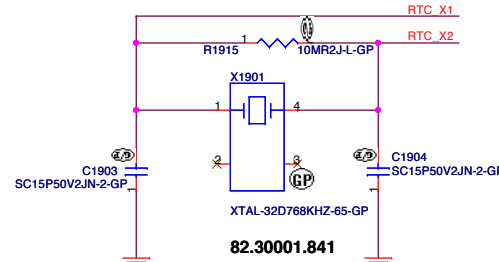
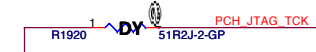
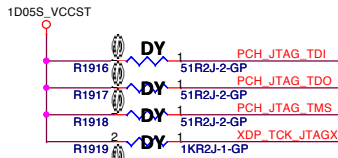
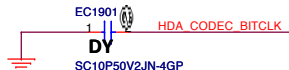
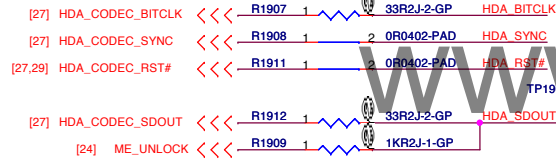


Layout: Place at the open door area.

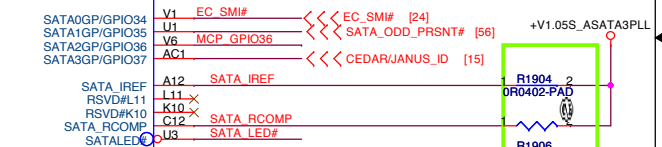
PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

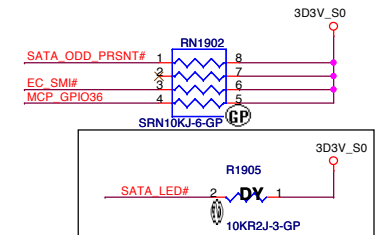
The internal pull-down is disabled after PLTRST# deasserts



HDD1
ODD



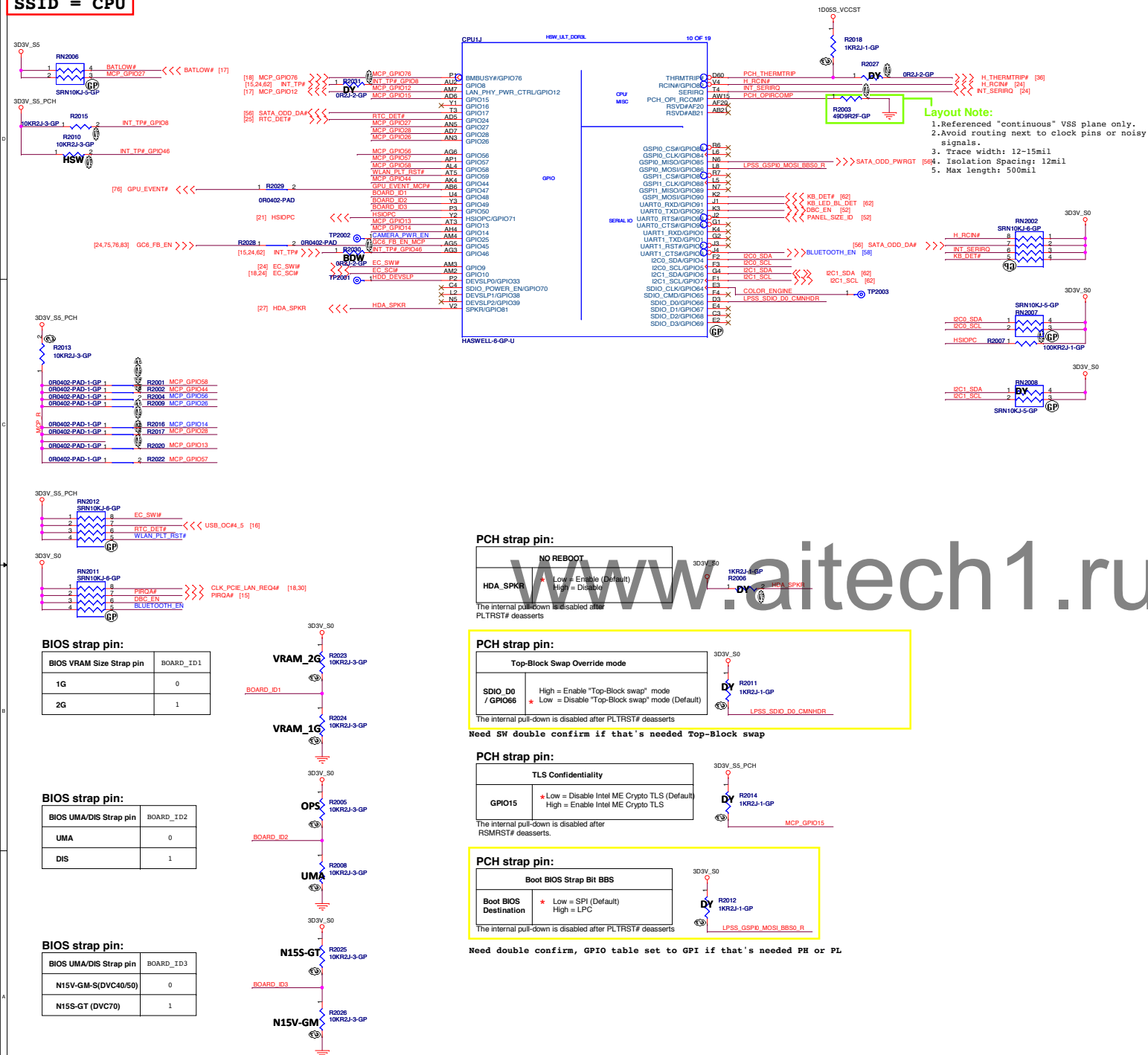
Layout Note:
4mil trace at break-out and 3
12-15mil trace with <0.2 ohms
and length total <= 500mils.

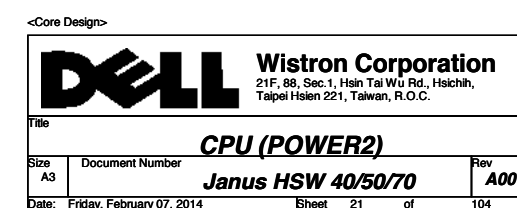


Unused SATA[3:0]GP pins must be terminated to either
3.3V rail or GND using 8.2K to 10K on the
motherboard. Either pull-up or pull-down is acceptable.

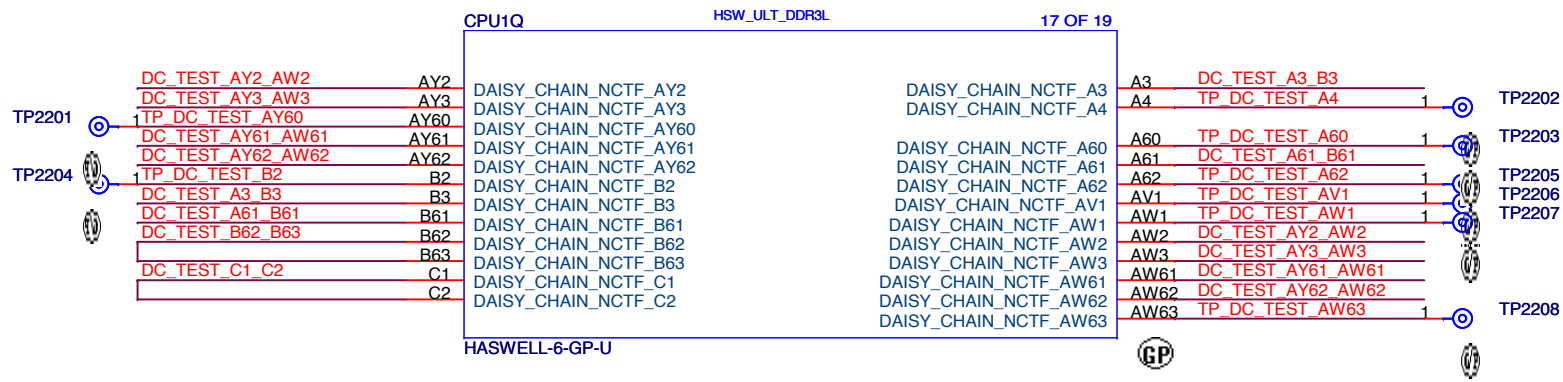
<Core Design>

SSID = CPU






SSID = PCH



<Core Design>



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Title

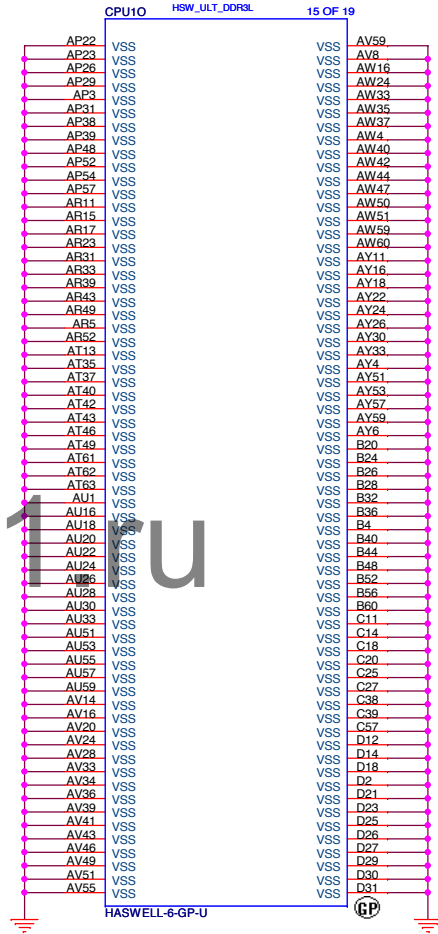
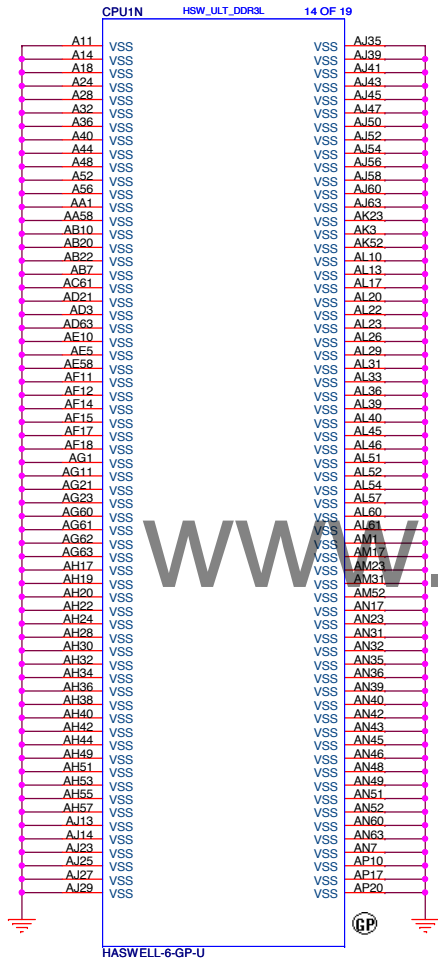
CPU (RSVD)

Size A4	Document Number Janus HSW 40/50/70	Rev A00
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SSID = PCH



<Core Design>



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Title

CPU(VSS)

Size
A3

Document Number

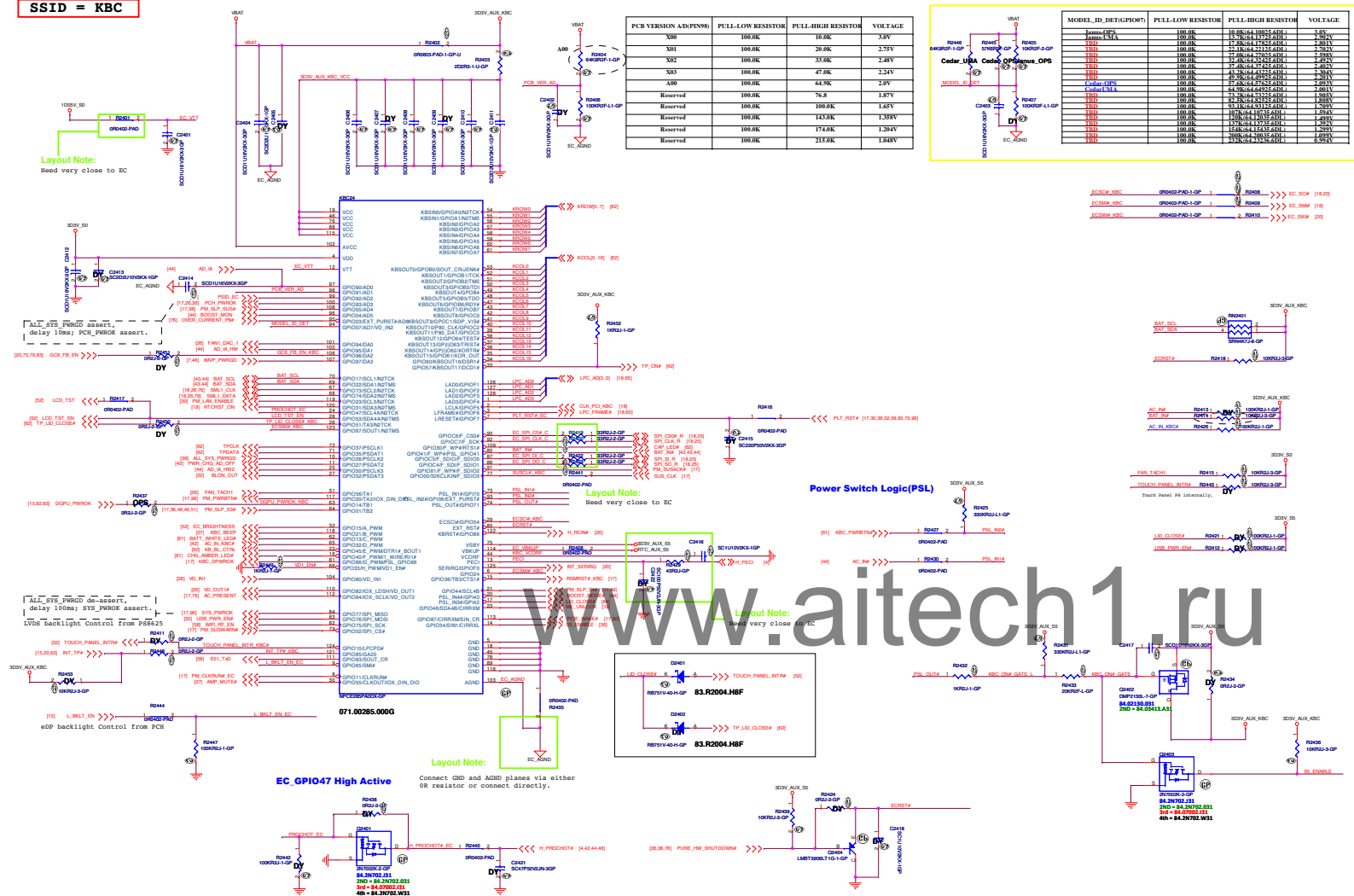
Janus HSW 40/50/70

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Date: Friday, February 07, 2014

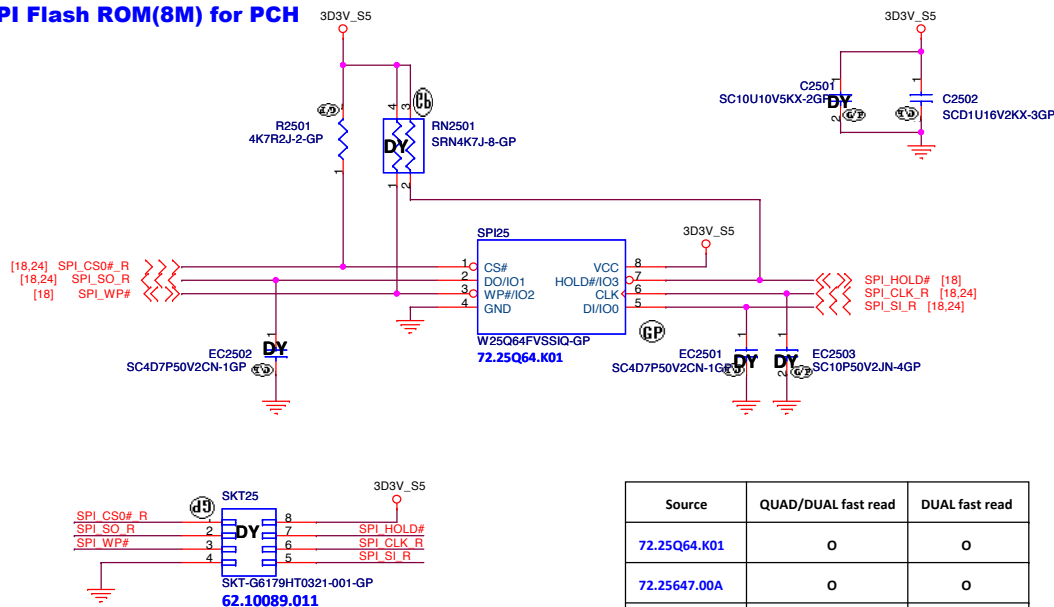
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SSID = KBC



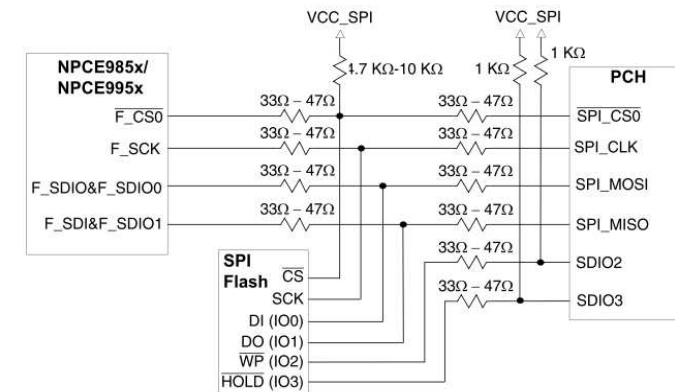
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



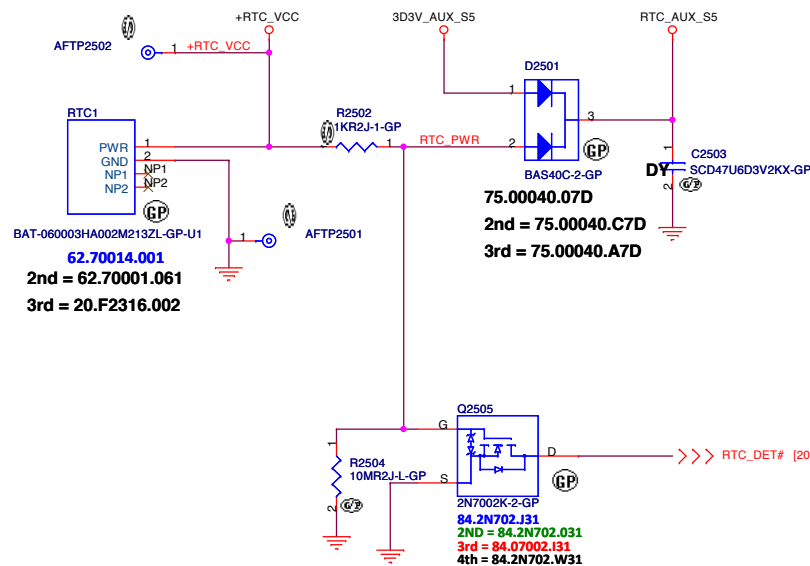
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o
072.25B64.0001	o	o

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



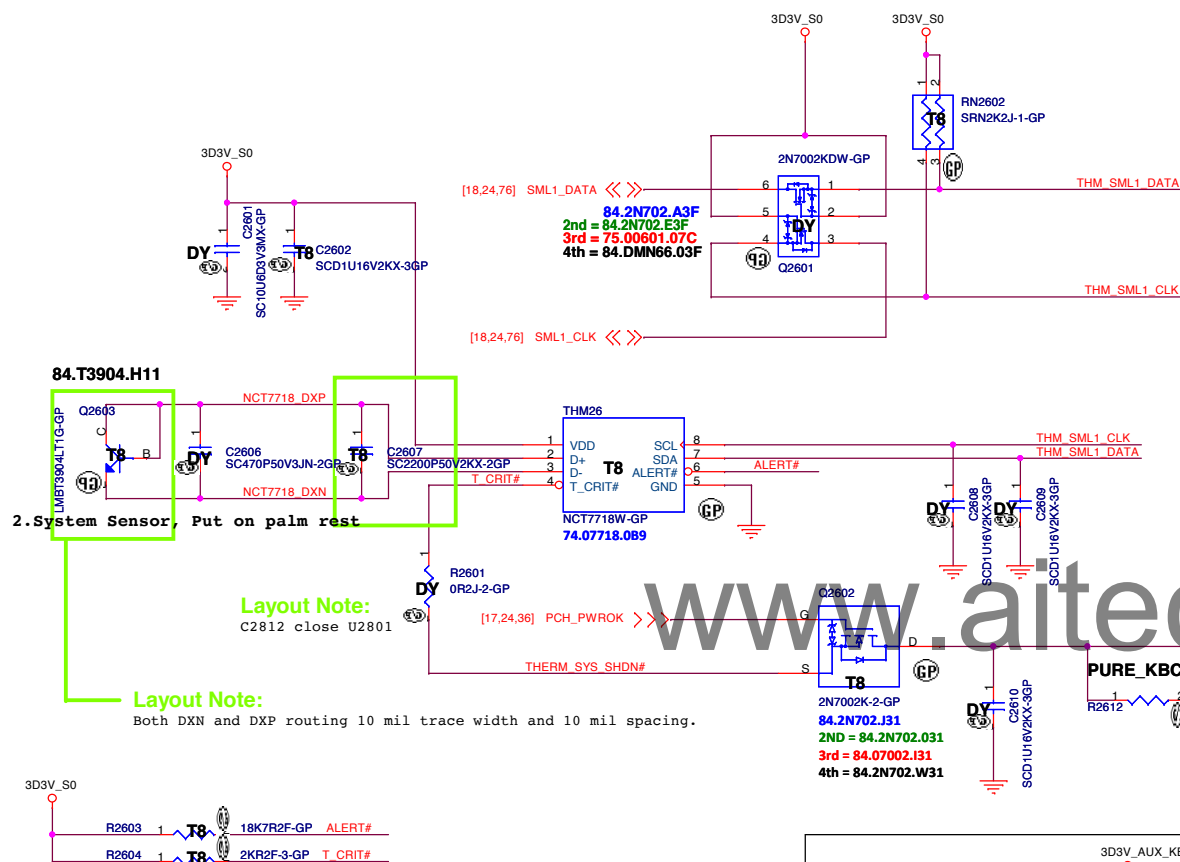
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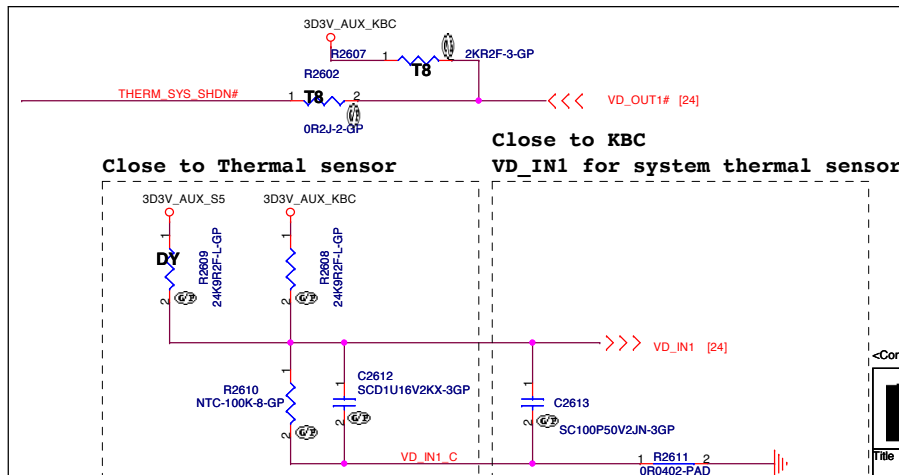
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Title	Flash/RTC		
Size	Document Number	Rev	
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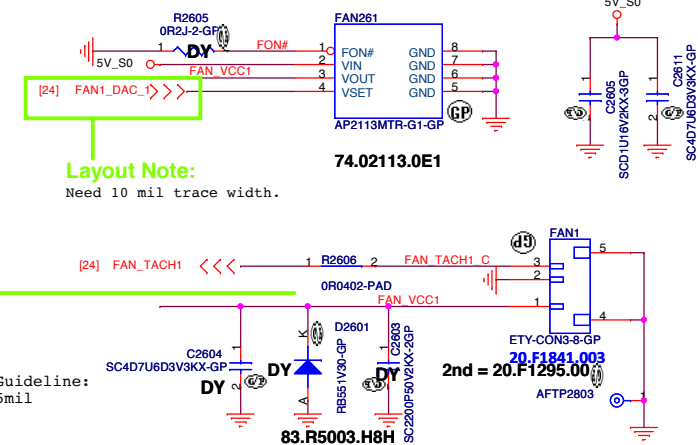
SSID = Thermal



TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



Fan controller1





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Document Number

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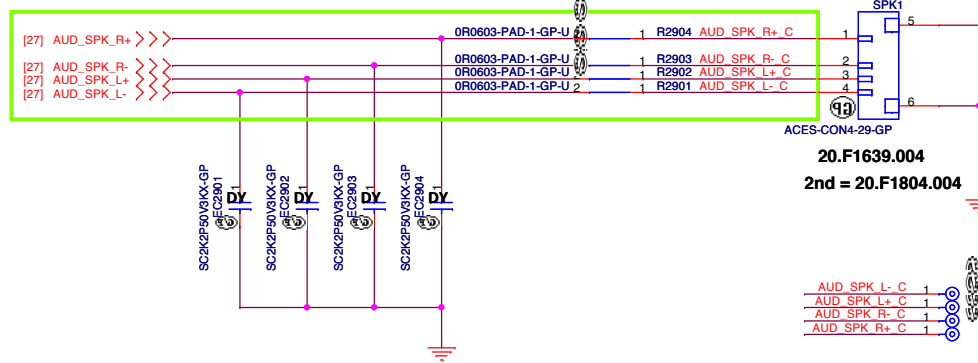
Date: Friday, February 07, 2014

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Layout Note:

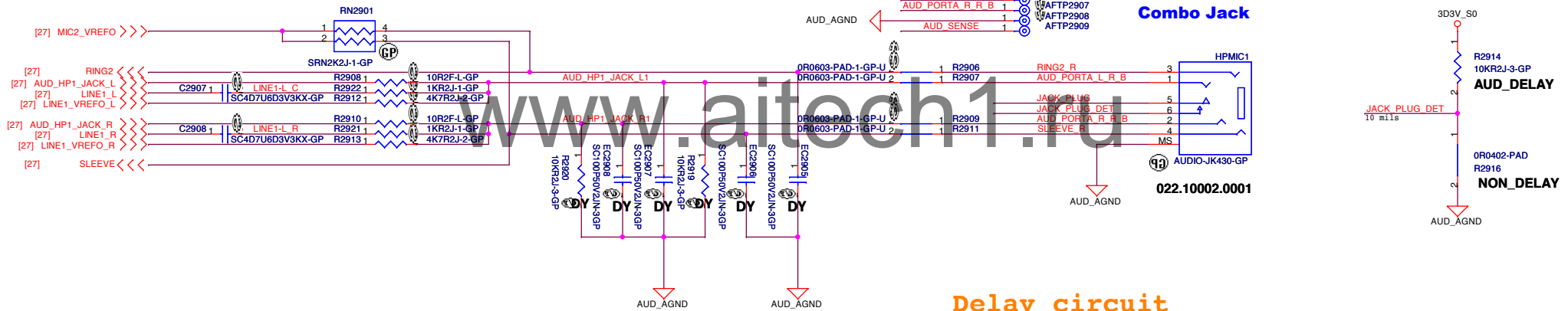
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

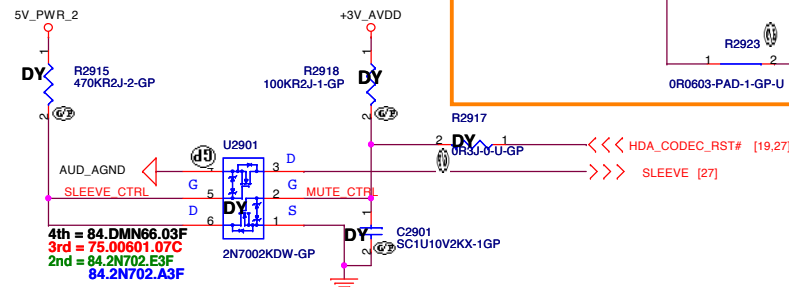
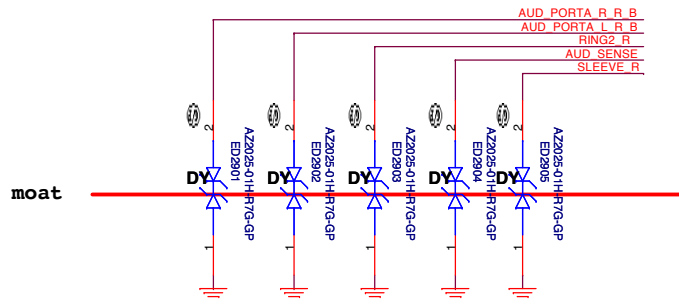
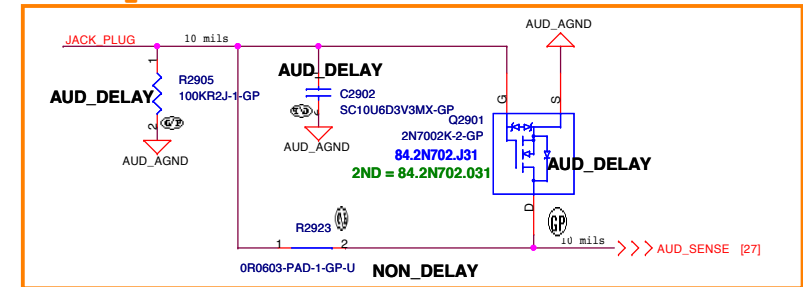


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

AUD_SPK_L- C 1 AFTP2901
 AUD_SPK_L+ C 1 AFTP2902
 AUD_SPK_R- C 1 AFTP2903
 AUD_SPK_R+ C 1 AFTP2904



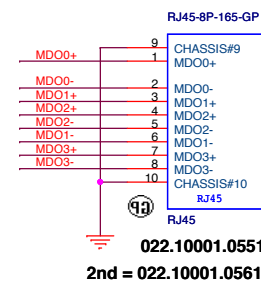
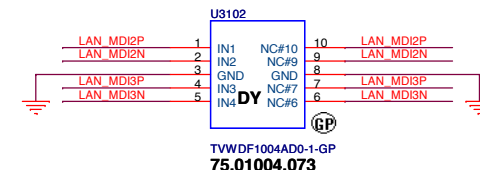
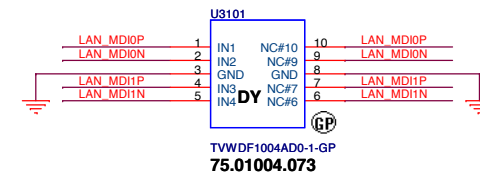
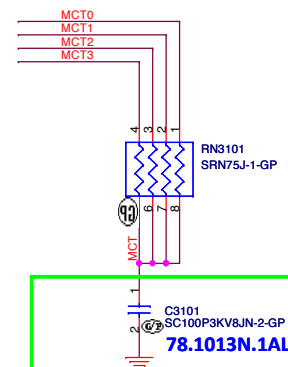
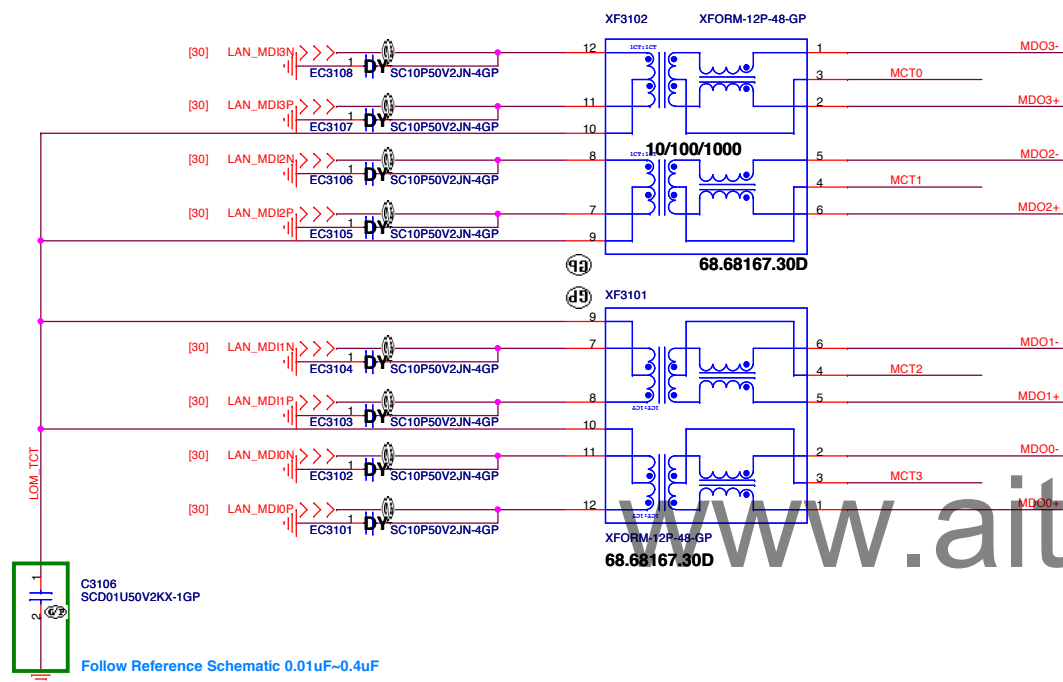
Delay circuit



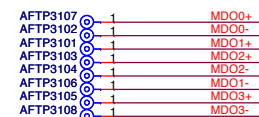
SSID = LOM

LAN TransFormer (10/100/1000M & 10/100M co-lay)

Layout note:
30 mil spacing between MDI differential pairs.



Layout:
Place near RJ45



<Core Design>



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Title			XFOM&RJ45	
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Title

(Reserved)Card Reader

Size
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Title

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Size
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Document Number

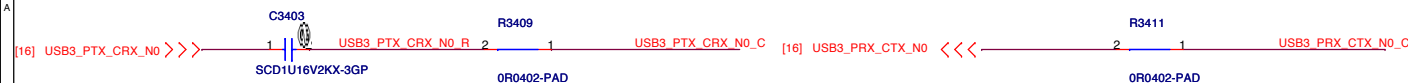
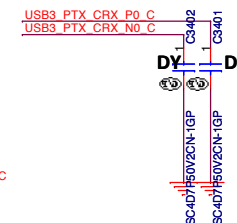
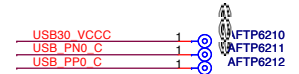
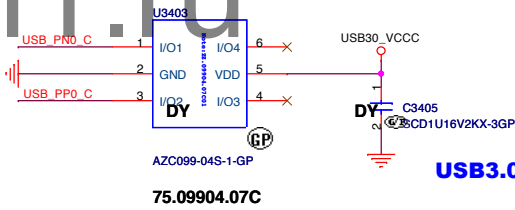
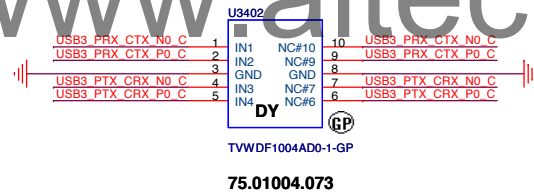
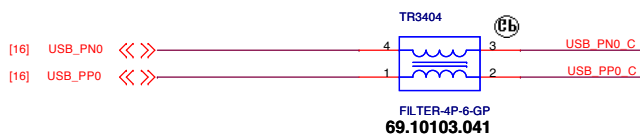
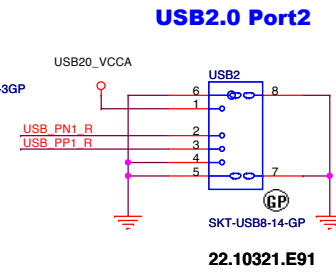
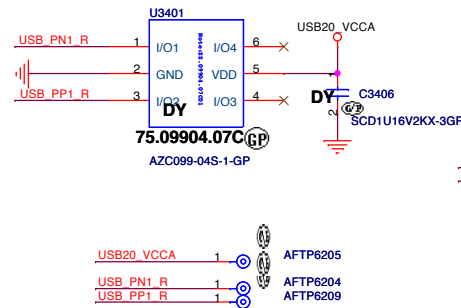
Janus HSW 40/50/70

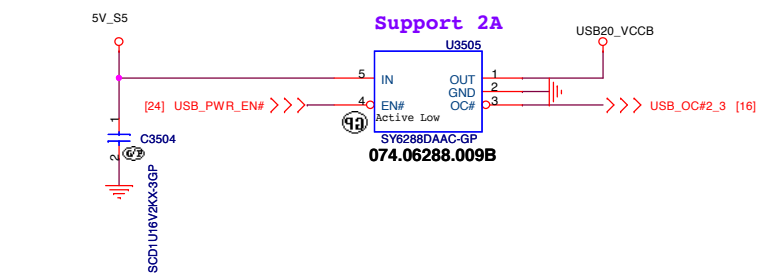
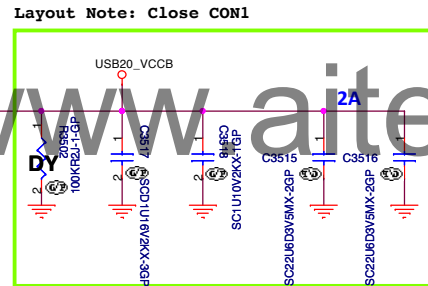
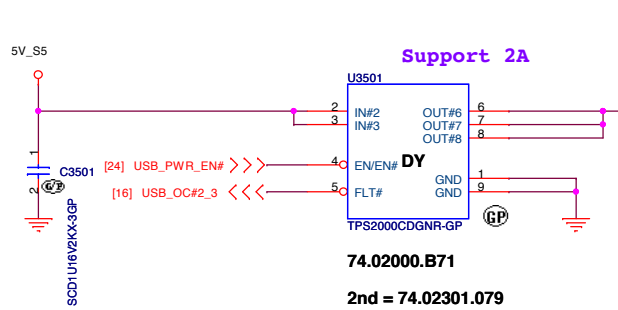
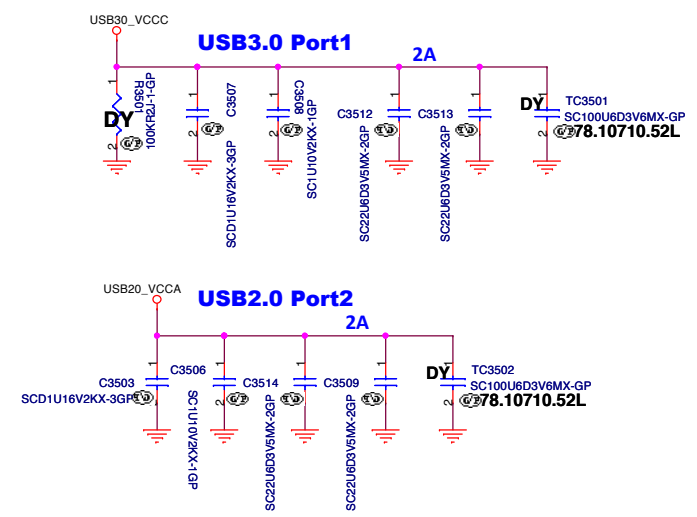
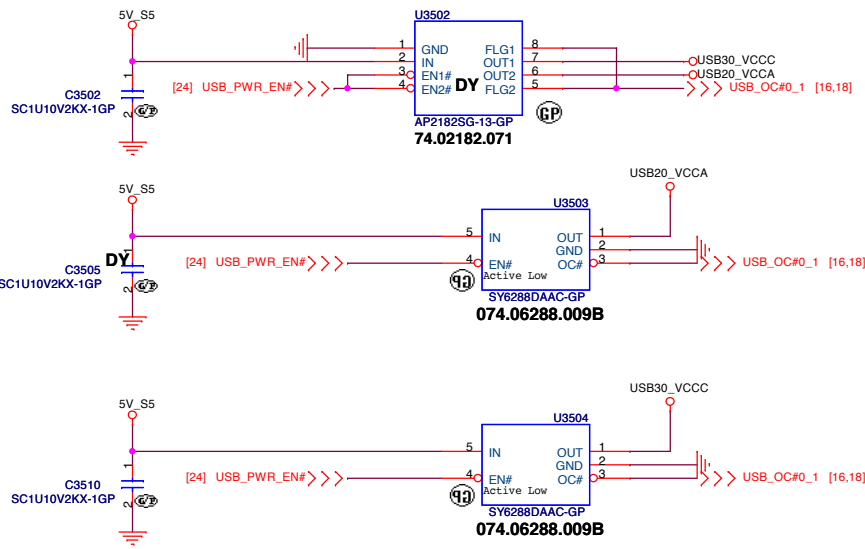
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SSID = USB

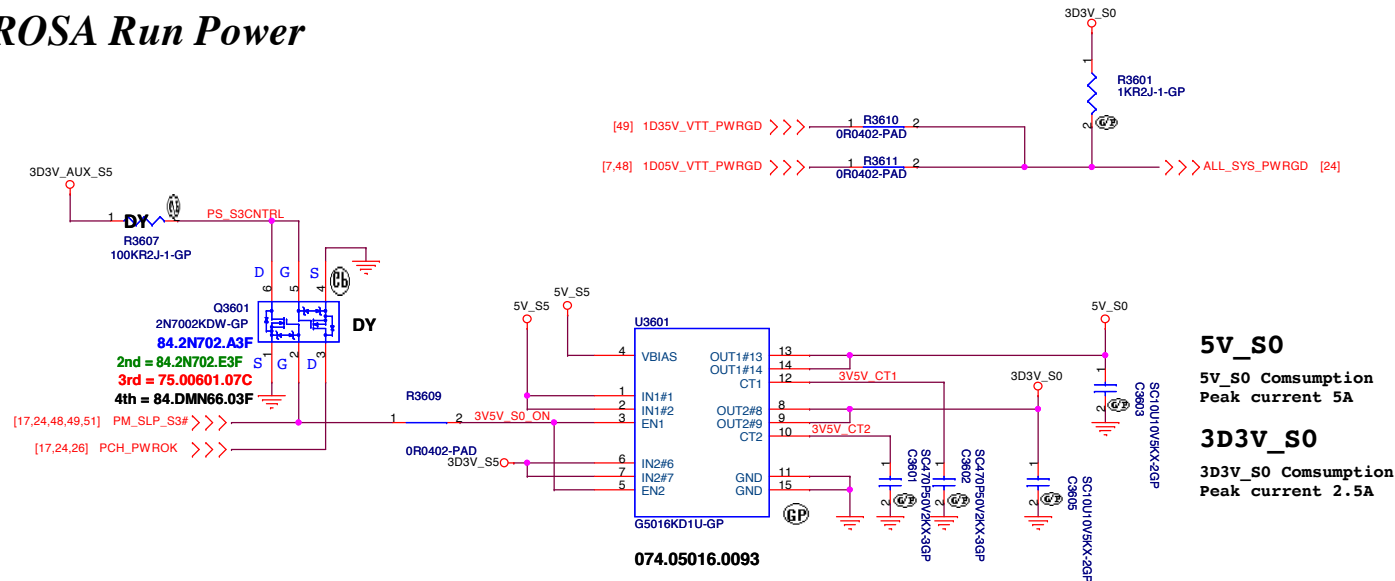




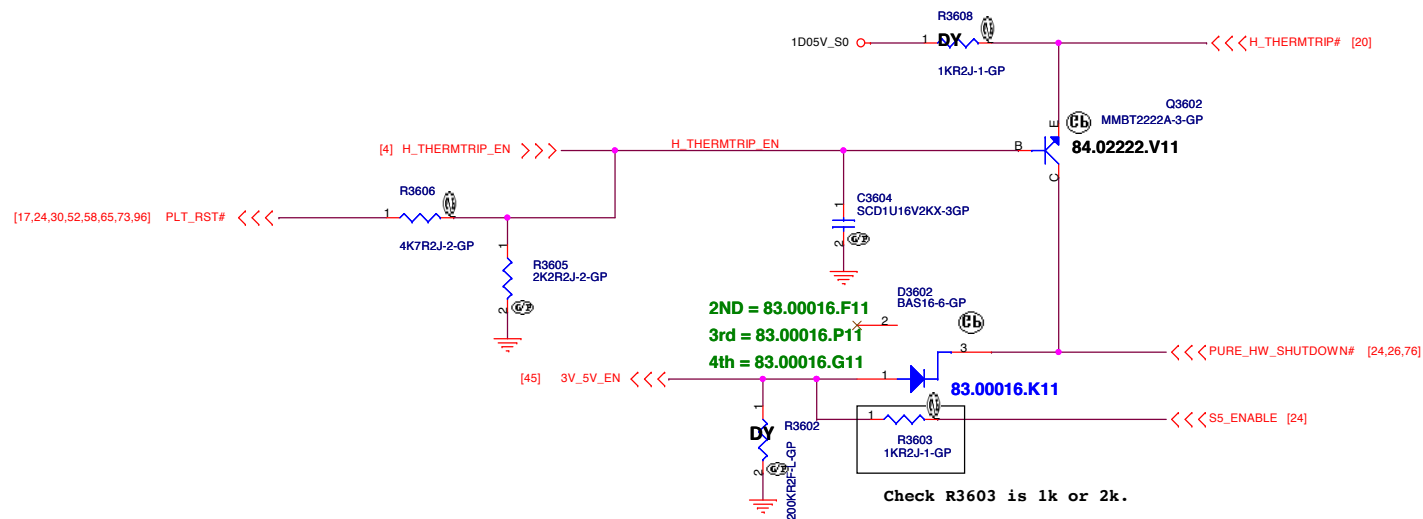
SSID = Reset.Suspend

Power Good

ROSA Run Power



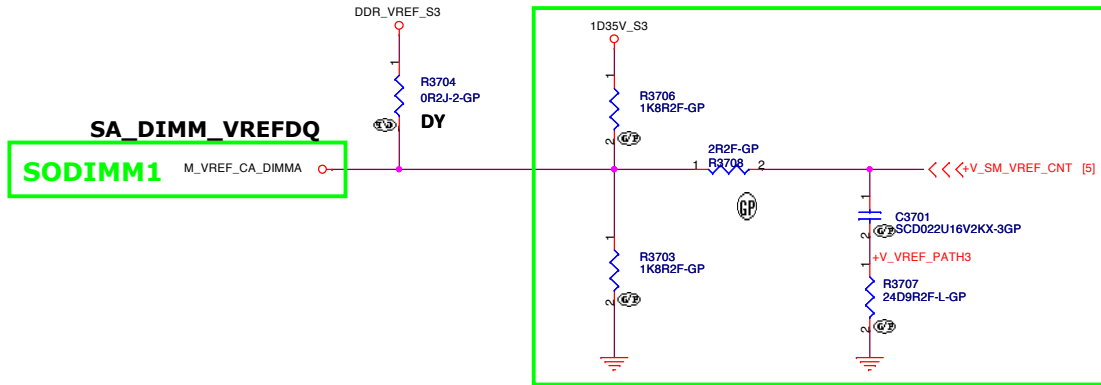
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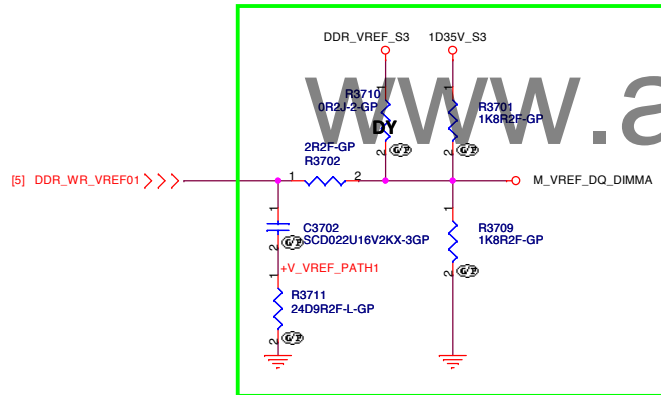
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SSID = Reset.Suspend

Layout Note:
Place Close SO-DIMM1



Layout Note:
Place Close SO-DIMM1



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Title

S3 Reduction Circuit

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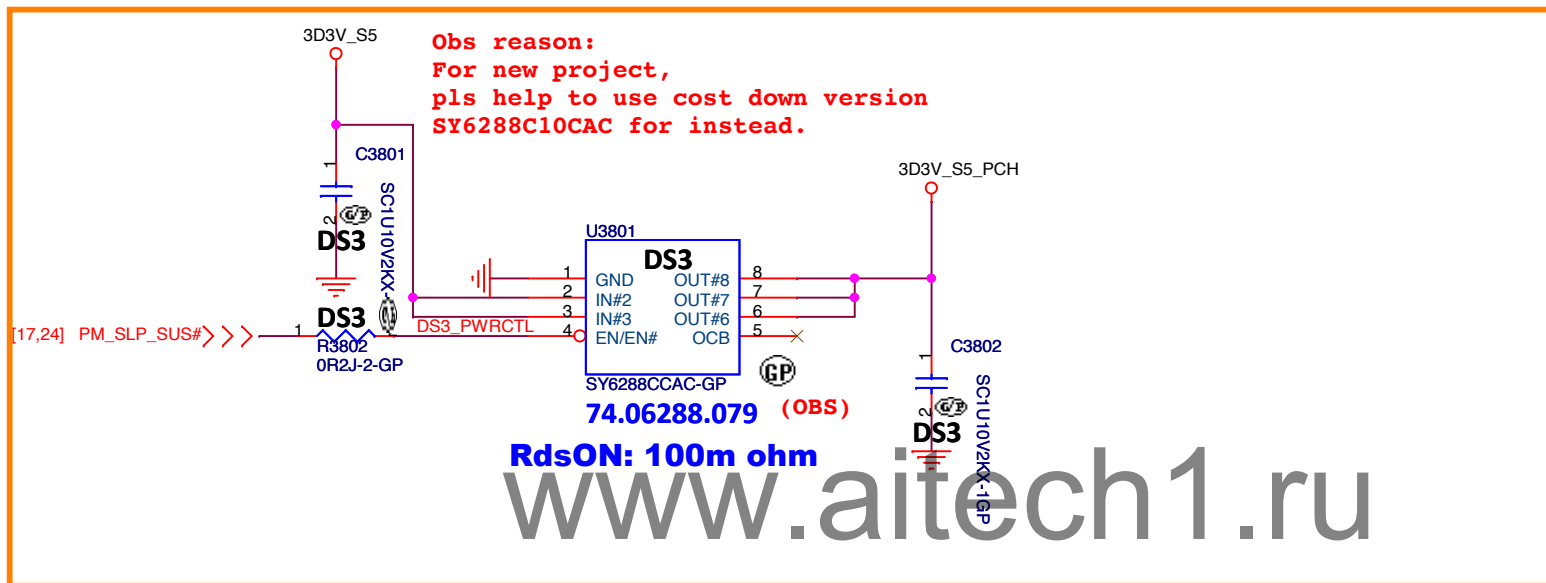
A00

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Obs reason:
For new project,
pls help to use cost down version
SY6288C10CAC for instead.



<Core Design>



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Title

DSW

Size
A4

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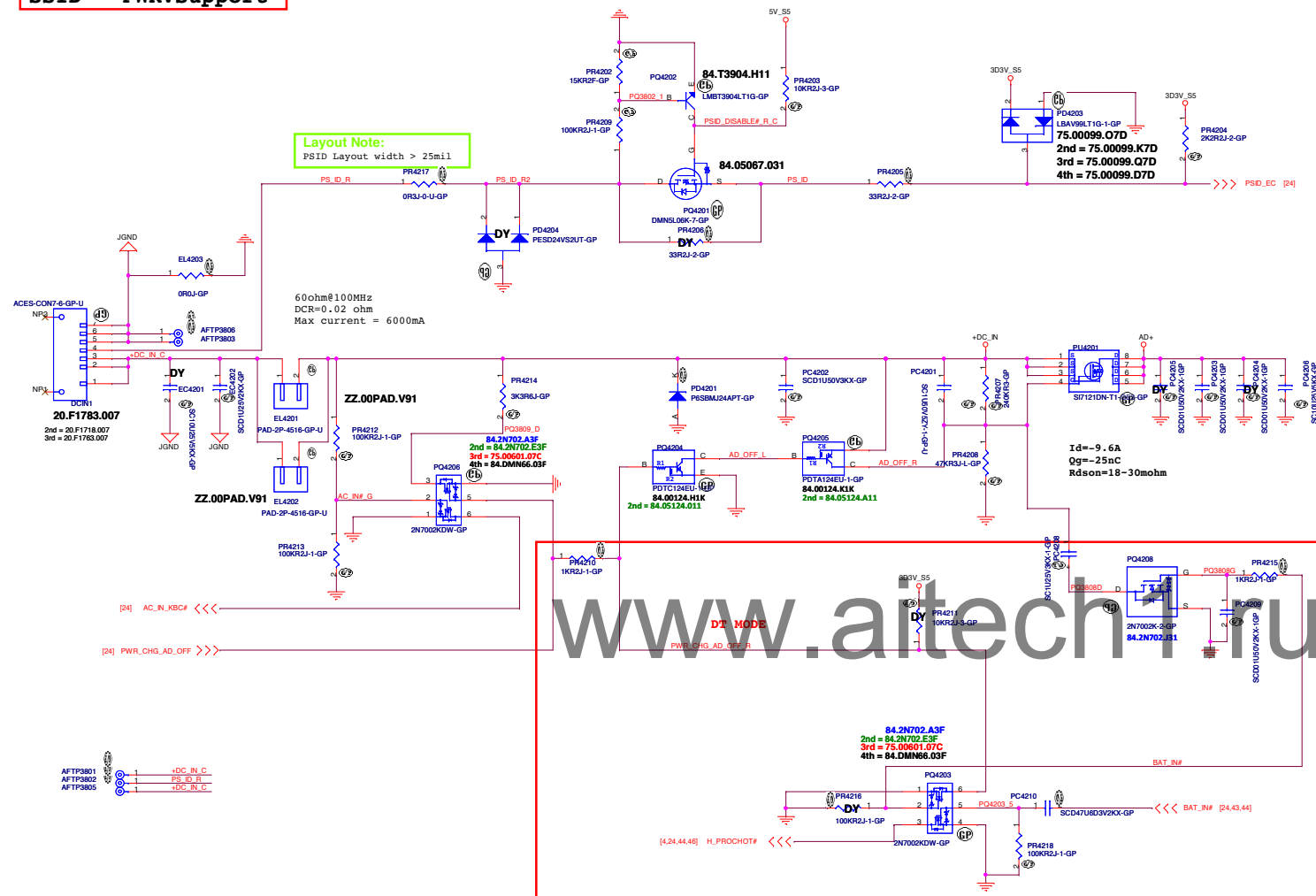
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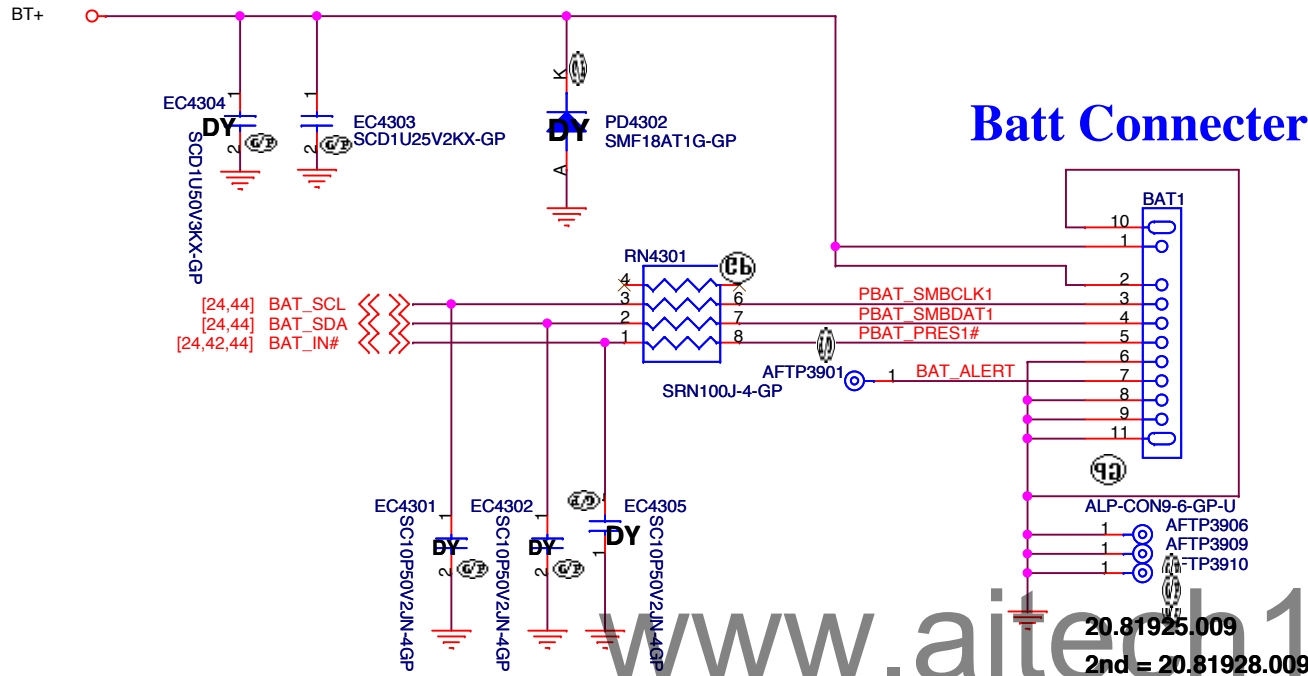
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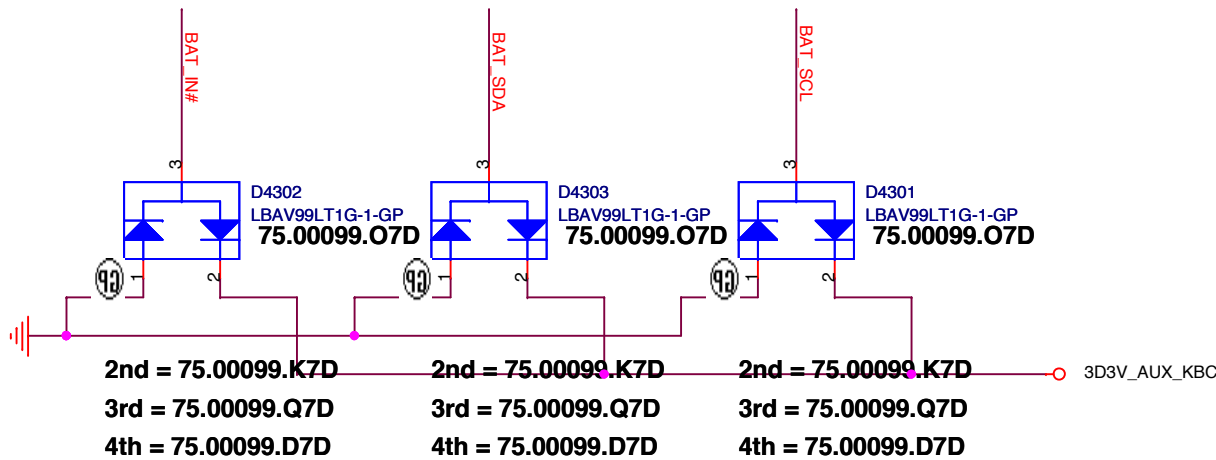
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<i>Reserved</i>			
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SSID = PWR.Support

SSID = PWR.Support



Placement: Close to Batt Connector



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BATT CONN

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Document Number

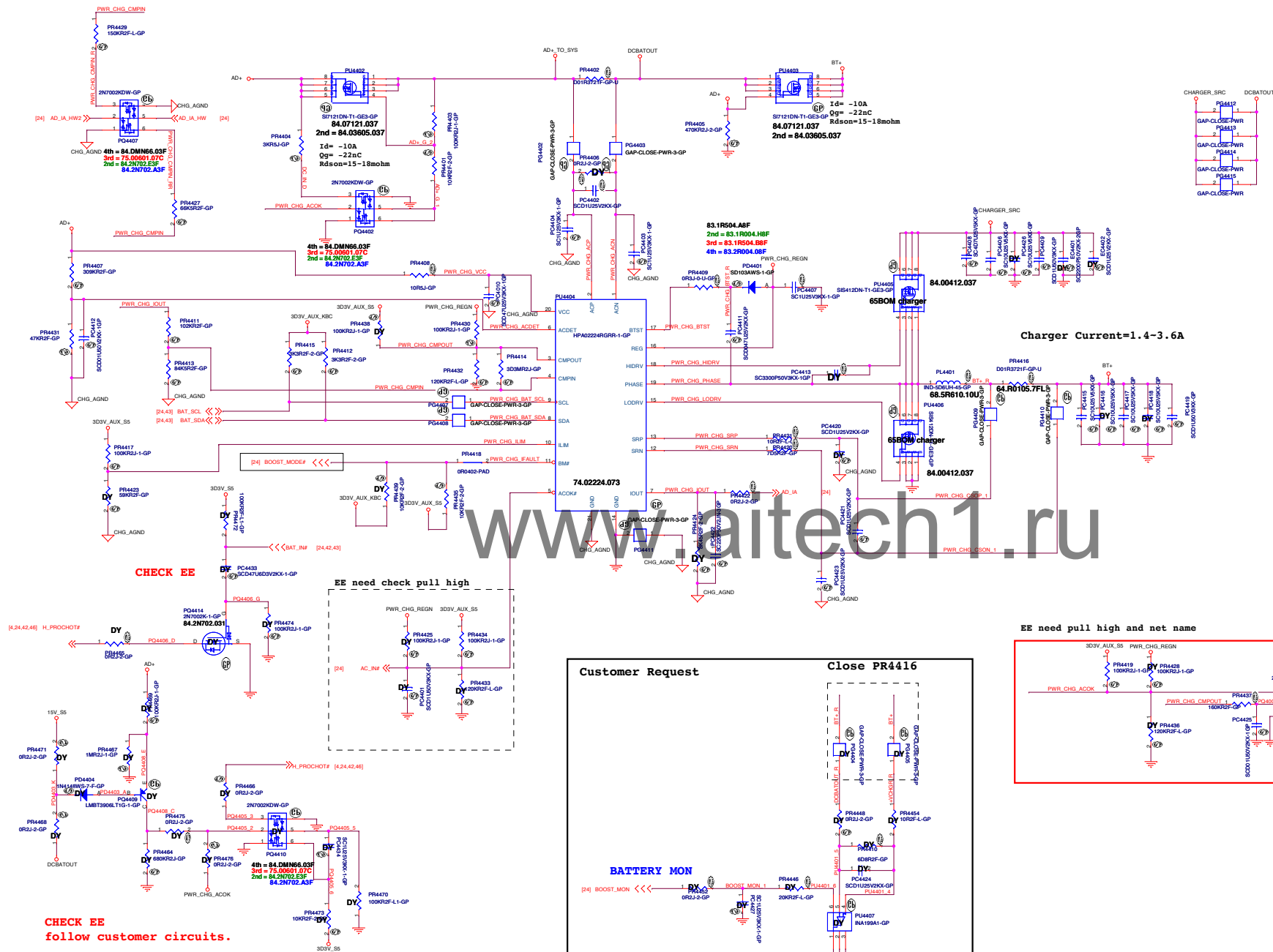
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Date: Friday, February 07, 2014

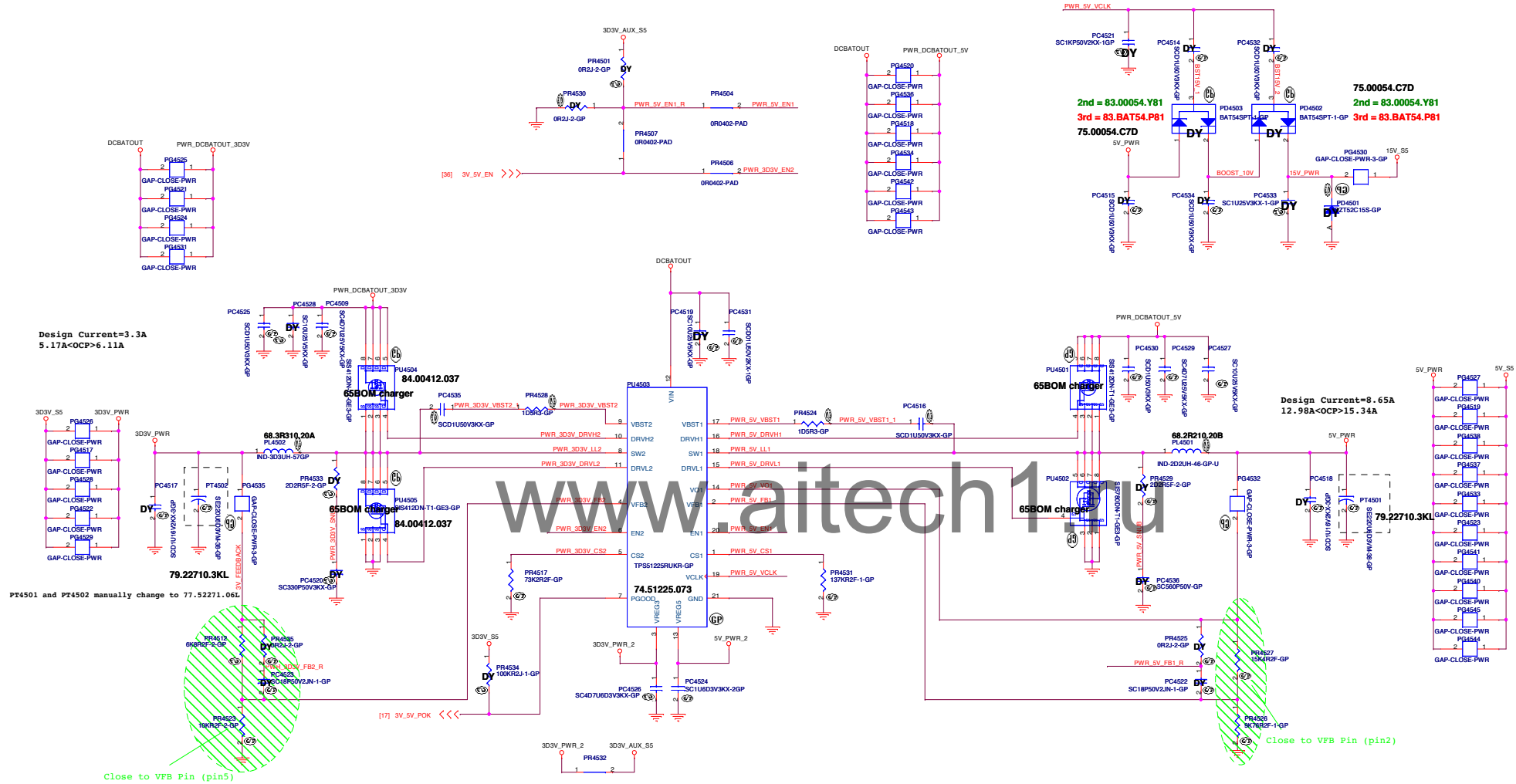
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SSID = Charger



H_PROCHOT#	AD_IA_HW	AD_IA_H
45W	0	0
65W	1	0
90W	0	1

SSID = PWR.Plane.Regulator_5v3p3v



Design Current=3.3A
5.17A<OCP>6.11A

Design Current=8.65A
12.98A<OCP>15.34A

PT4501 and PT4502 manually change to 77.52271.06L

Close to VFB Pin (pin5)

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

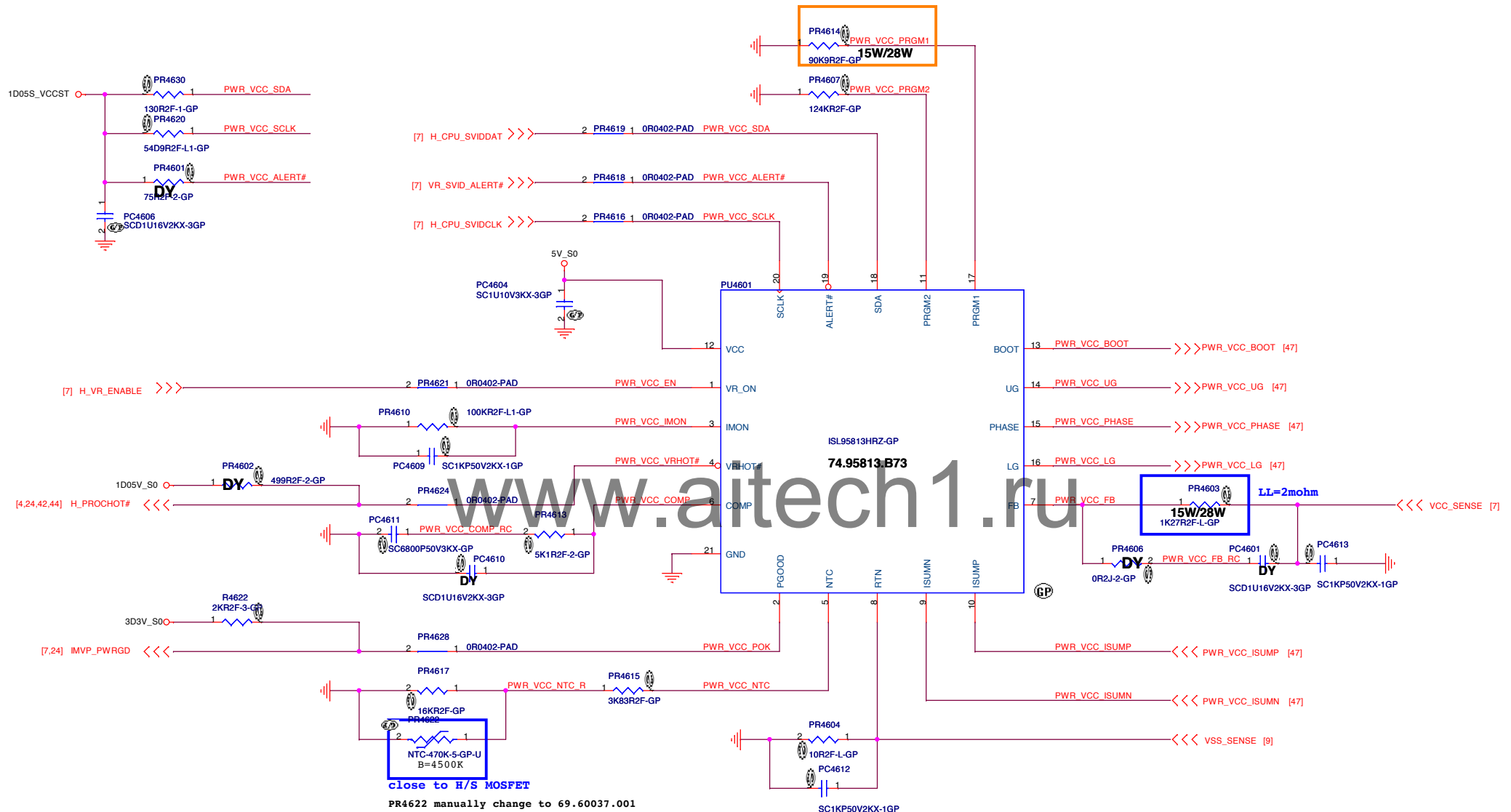
TPS51225 & TPS51285 Co-Lay

	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOK 2.2UH PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

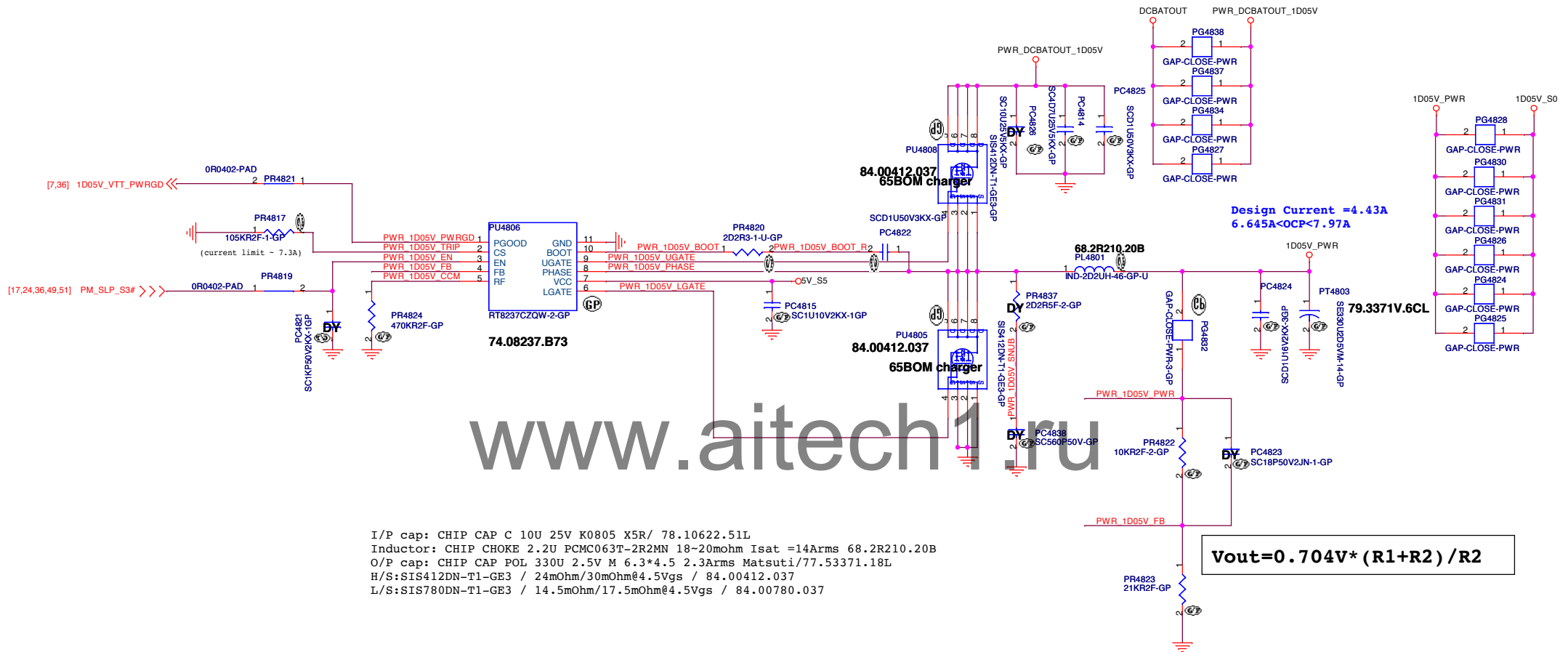
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SSID = CPU.Regulator



	PR4603	PR4614
15W	1.27K 64.12715.6DL	90.9K 64.90925.6DL
28W	1.58K 64.15815.6DL	113K 64.11335.6DL

SSID = PWR.Plane.Regulator_1p05v



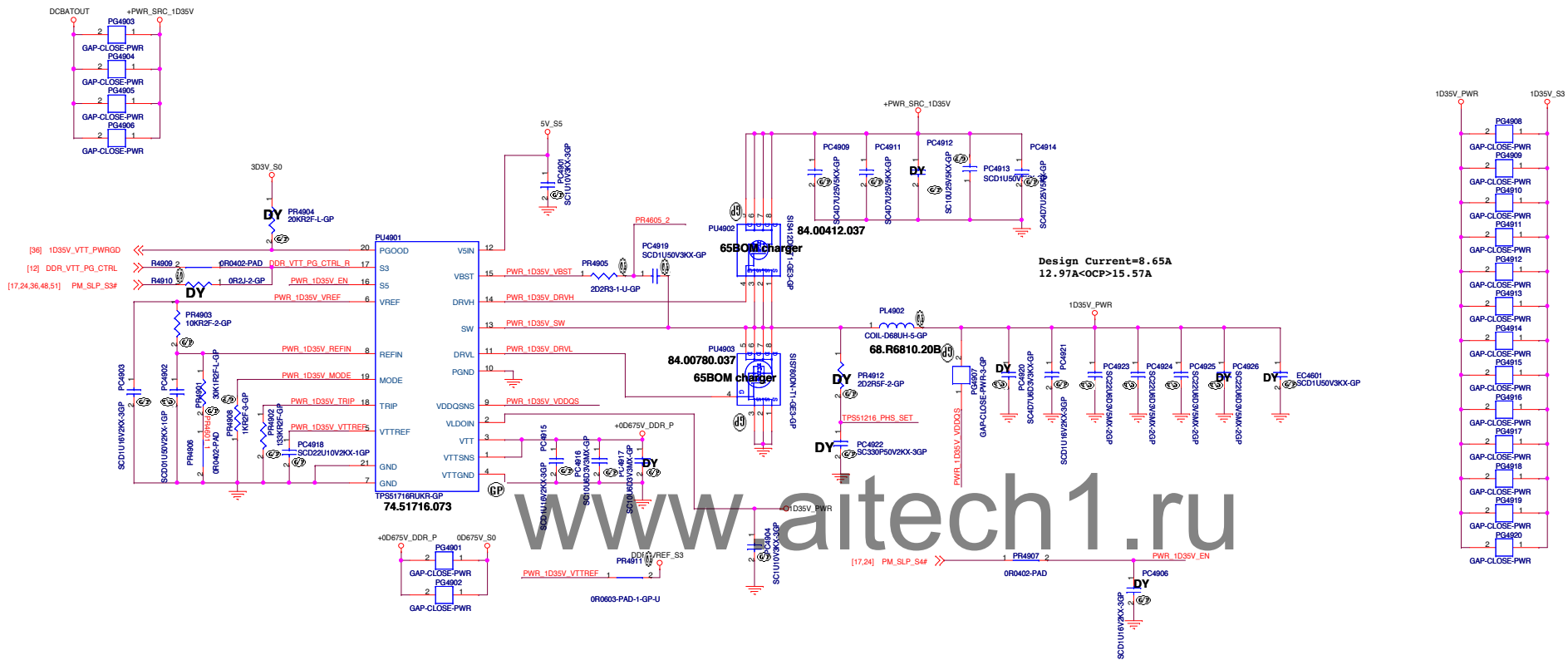
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$

<Core Design>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RT8237_1D05V			
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SSID = PWR.Plane.Regulator lp35v0p675v




State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP IND 0.1uH M PCMC0637-R104M 1.5~1.7mohm Isat =60Arms 68.R1010.10T
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3+4.5 2.3Arms Matsuti/77.53371.18L
 MOS: FET MOS FDM3364S NC POWER56 / 84.03664.037 / Q1: 8.5~11mohm @Vgs=4.5V Q2: 2.6~3.2mohm @Vgs=4.5V

<Core Design>

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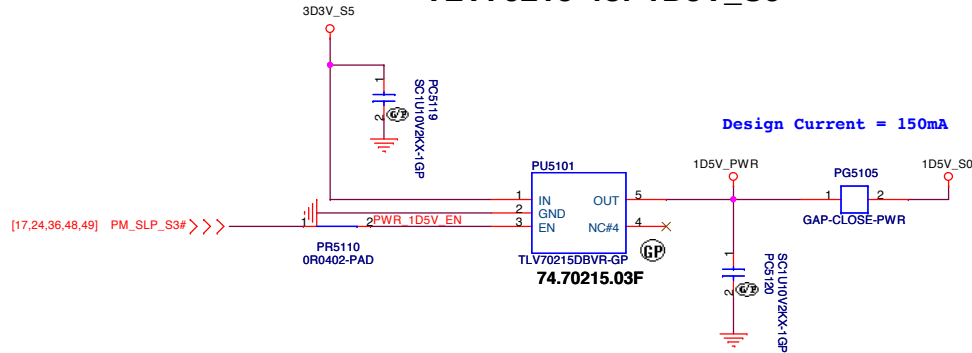
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Size A3	Document Number Janus HSW 40/50/70	Rev A00
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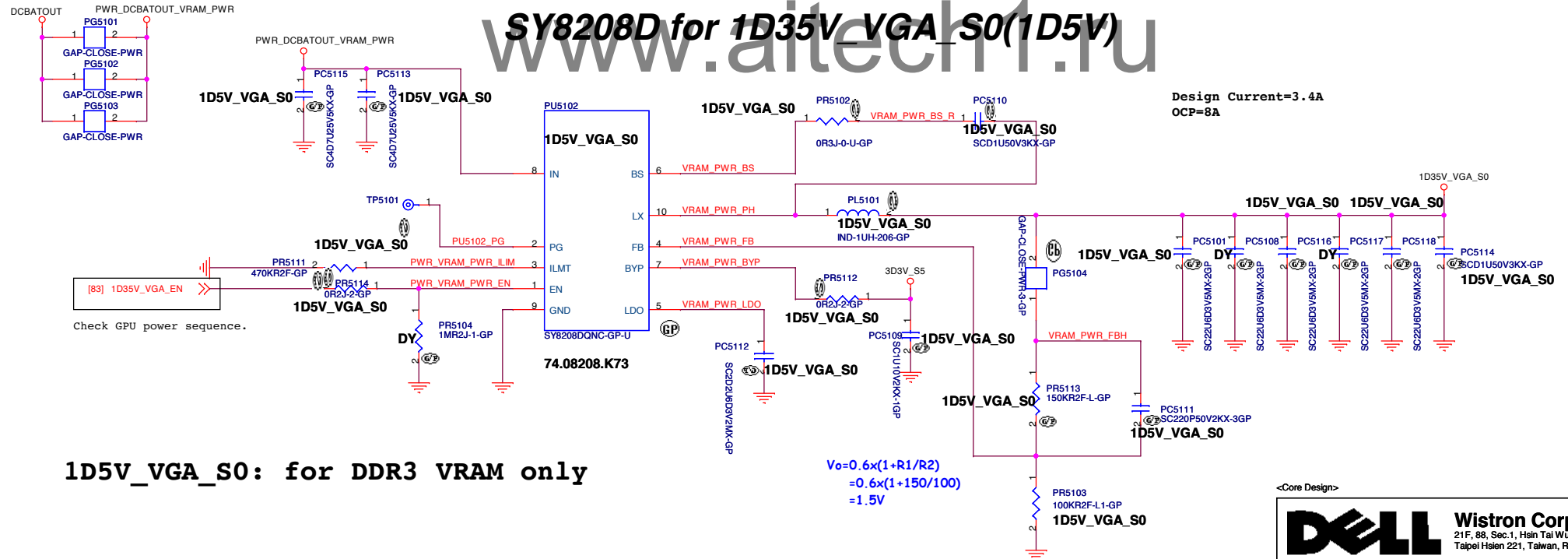
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SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0



SY8208D for 1D35V_VGA_S0(1D5V)



1D5V_VGA_S0: for DDR3 VRAM only

$$V_o = 0.6 \times (1 + R1/R2) = 0.6 \times (1 + 150/100) = 1.5V$$

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Title

HDMI Level Shifter/Connector

Size A3	Document Number Janus HSW 40/50/70	Rev X02
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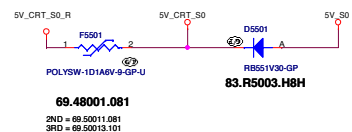
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The diagram shows the SCDD01U1H8V2KX-1-GP connector on the left and the CRT board connector on the right. The connections are as follows:

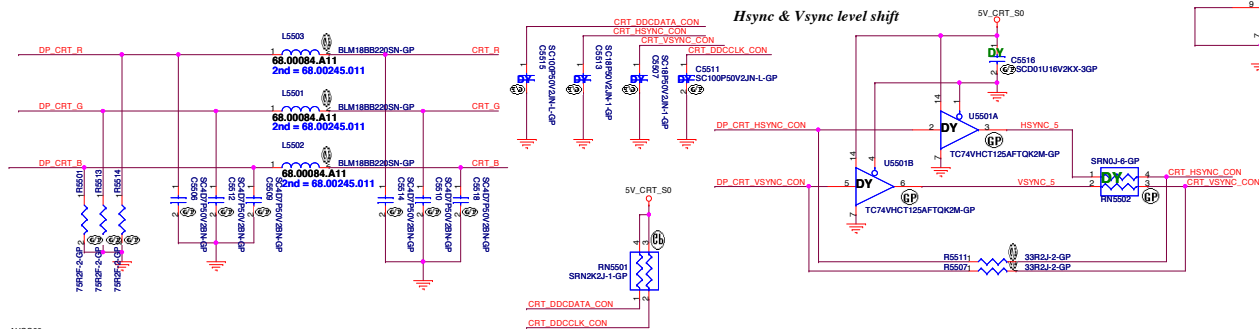
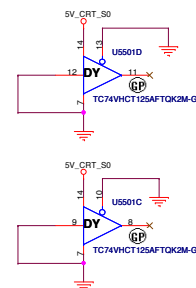
- Pin 1:** VCC_CRT_S0_R (5V1) to VCC_CRT (pin 9).
- Pin 2:** CRT_D0CDA_DATA_CON to D0CDA_DATA_ID1 (pin 12).
- Pin 3:** CRT_D0CLK to D0CLK_ID3 (pin 13).
- Pin 4:** CRT_A to GND (pin 5).
- Pin 5:** CRT_B to GND (pin 6).
- Pin 6:** CRT_C to GND (pin 7).
- Pin 7:** CRT_D to GND (pin 8).
- Pin 8:** CRT_VSYNC_CON to VSYNC (pin 14).
- Pin 9:** CRT_HSYNC_CON to HSYNC (pin 15).

Additional labels on the CRT board include:

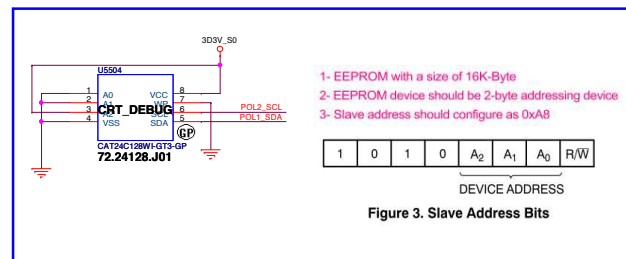
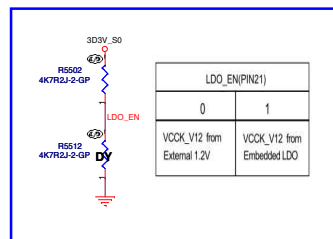
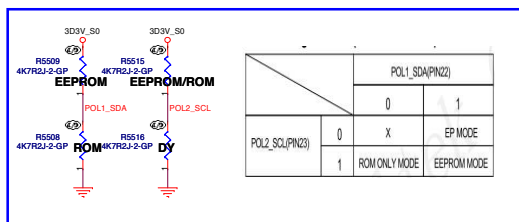
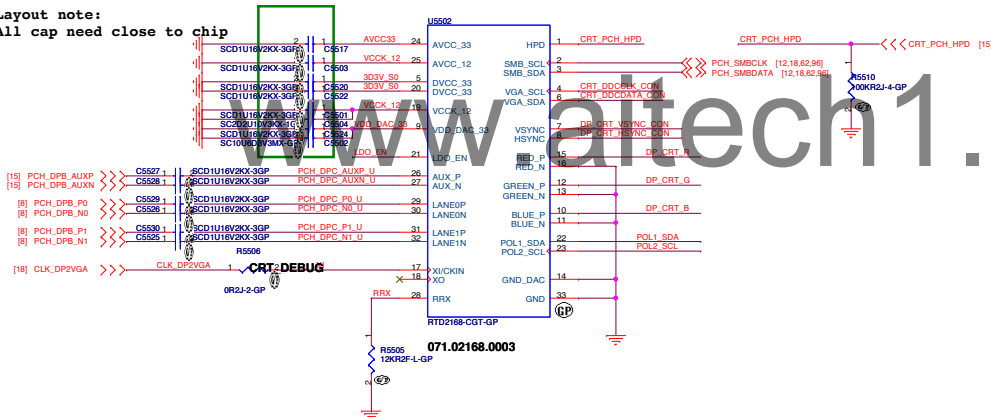
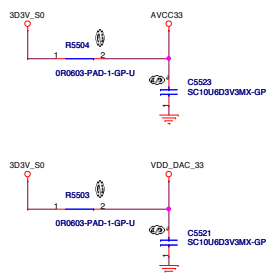
- NC4:** NC4F11 (pins 4 and 11).
- NC5:** GND (pins 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15).
- Bottom Label:** D-SUB-15-252-GP



CRT RGB
CRT H/VSYNC
CRT SMBUS

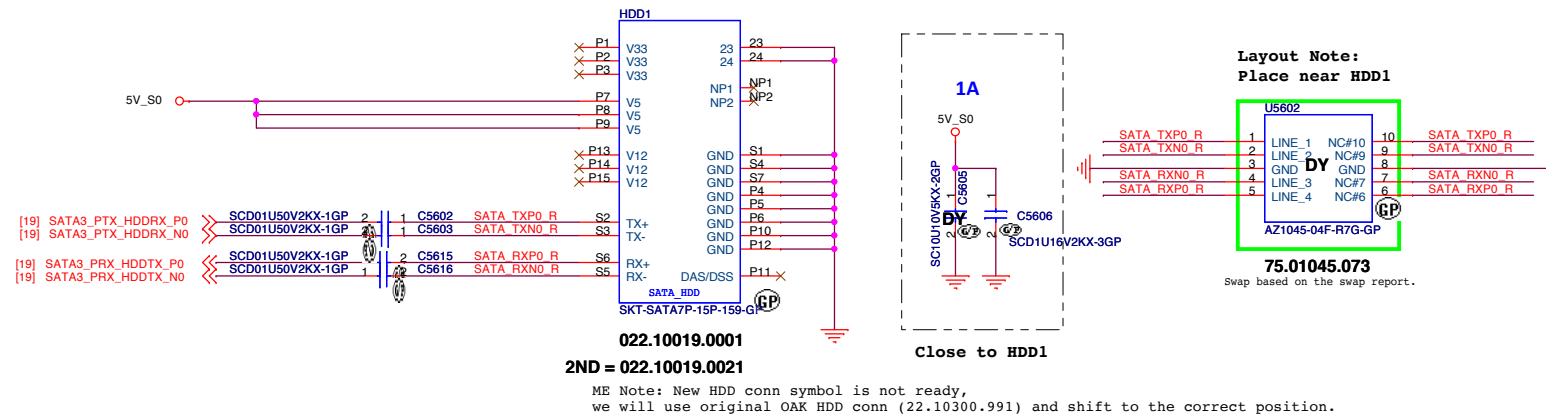


Layout note:
All cap need close to chip

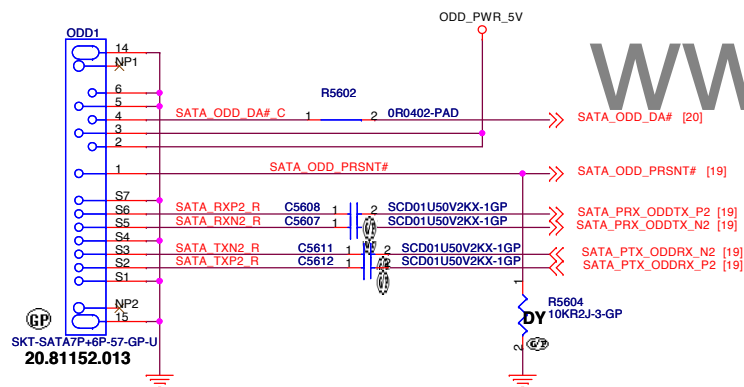


SSID = SATA

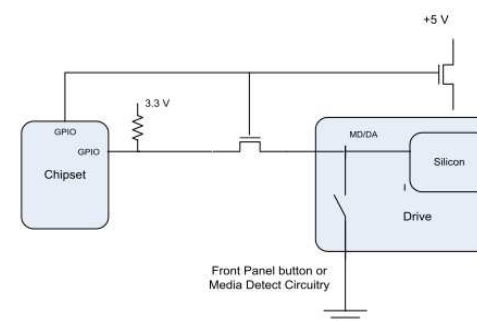
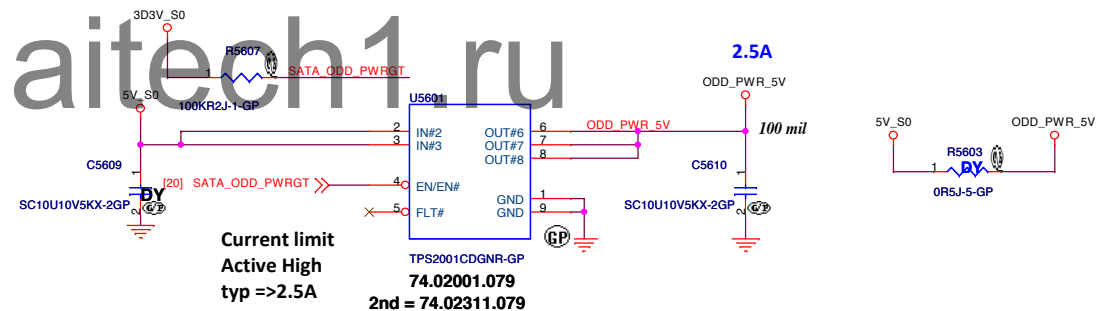
SATA HDD Connector



ODD Connector



SATA Zero Power ODD



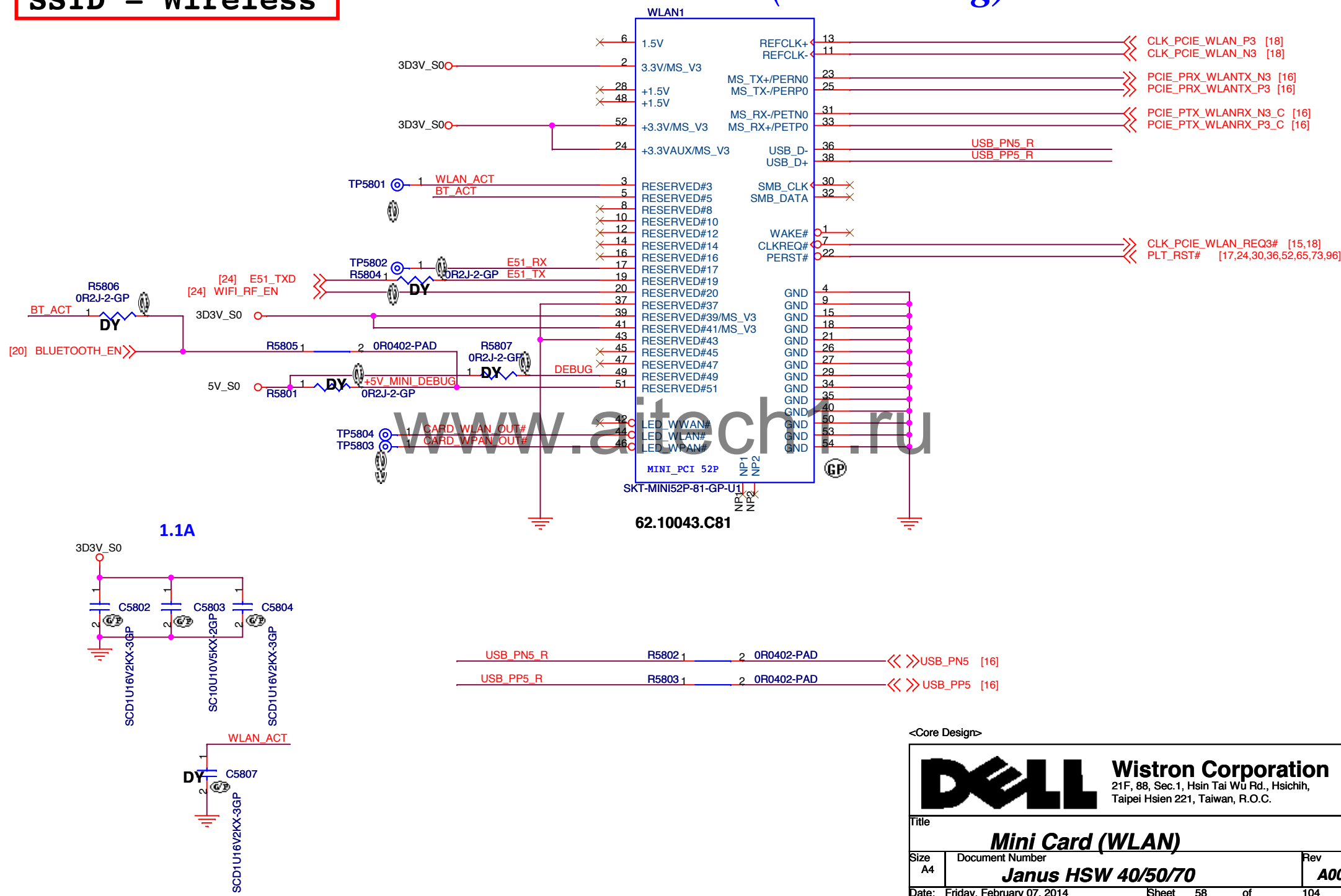
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SSID = ESATA

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SSID = Wireless

Mini Card Connector(802.11a/b/g)



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Title

Mini Card (WLAN)

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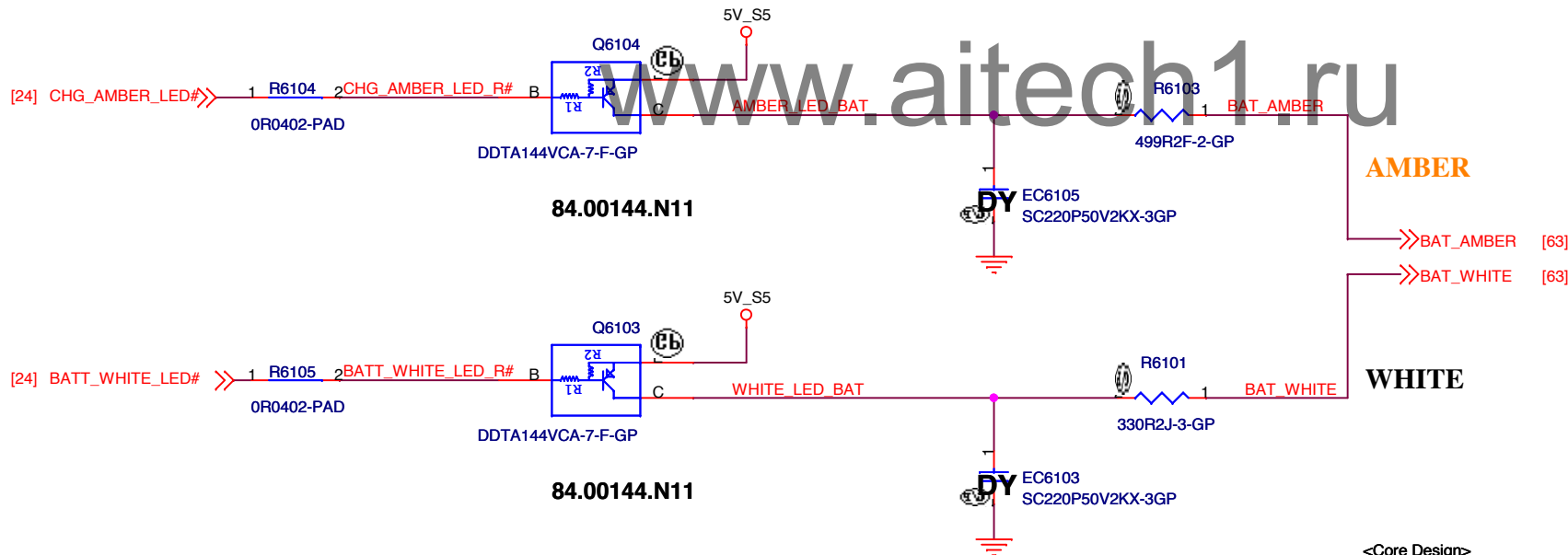
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SSID = User.Interface

Power button

Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

<Core Design>

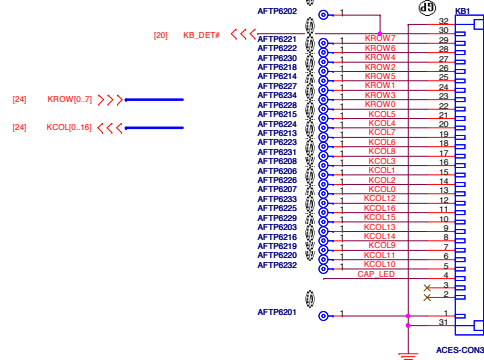


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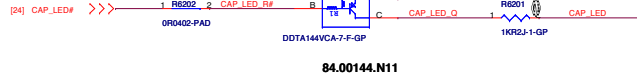
Title			LED Bard/Power Button	
Size	Document Number		Rev	
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SSID = KBC

Internal Keyboard Connector (DVC40)

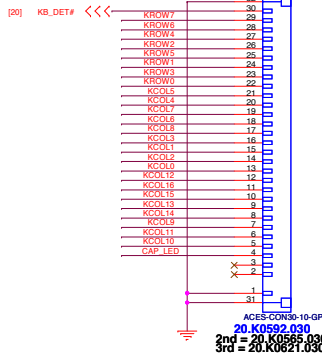


CAP LED Control LOW acted from KBC GPIO



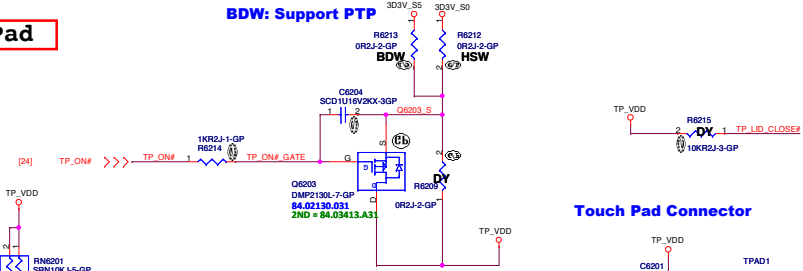
84.00144.N11

Internal Keyboard Connector (DVC50/DVC70)



SSID = Touch.Pad

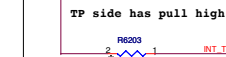
BDW: Support PTP



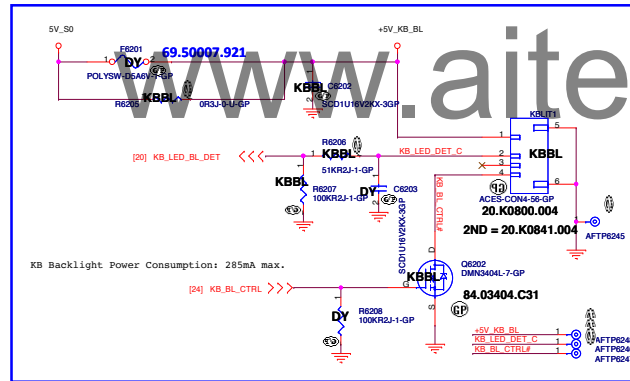
Touch Pad Connector

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

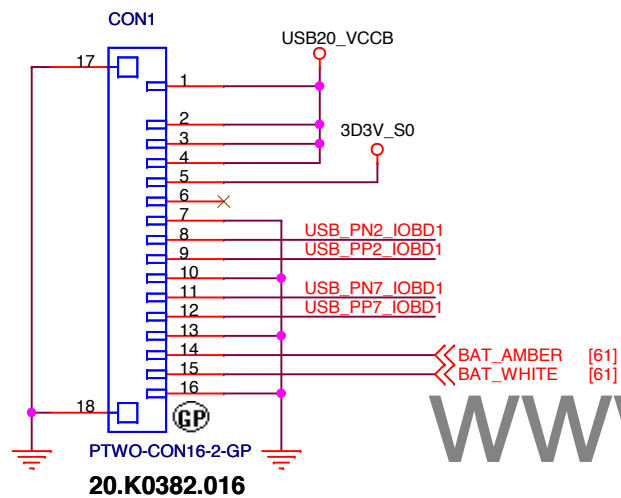
Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



Keyboard Backlight (DVC70)

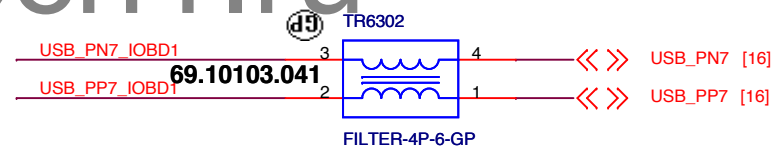
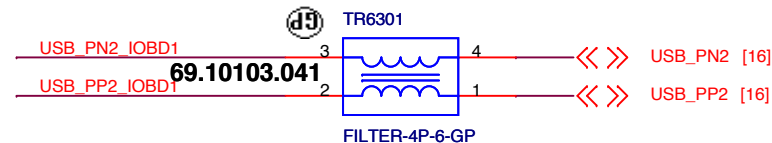


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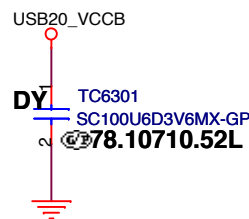


USB2.0 Port3 Card Reader LED

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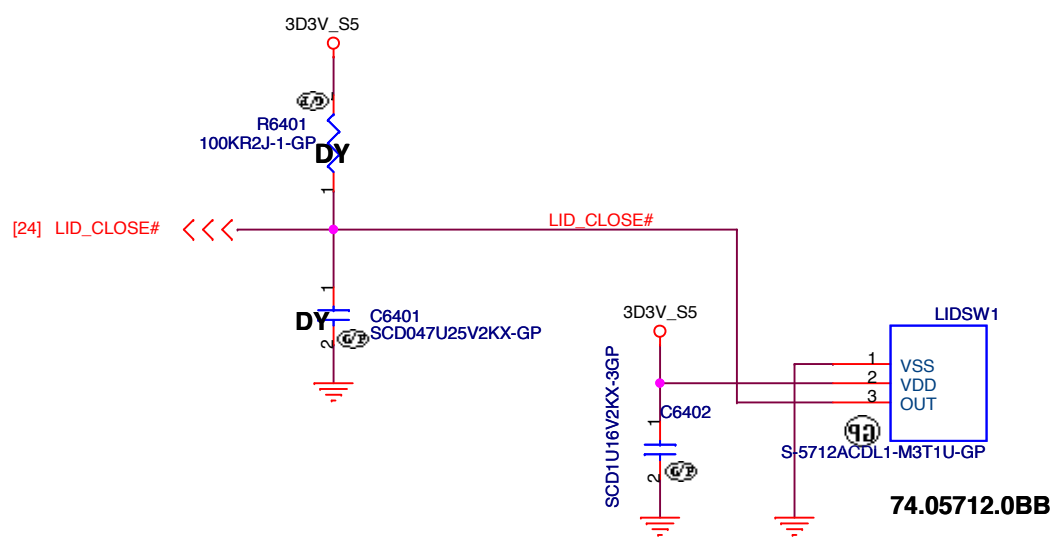
The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



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		Title IO Board Connector	
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SSID = User.Interface

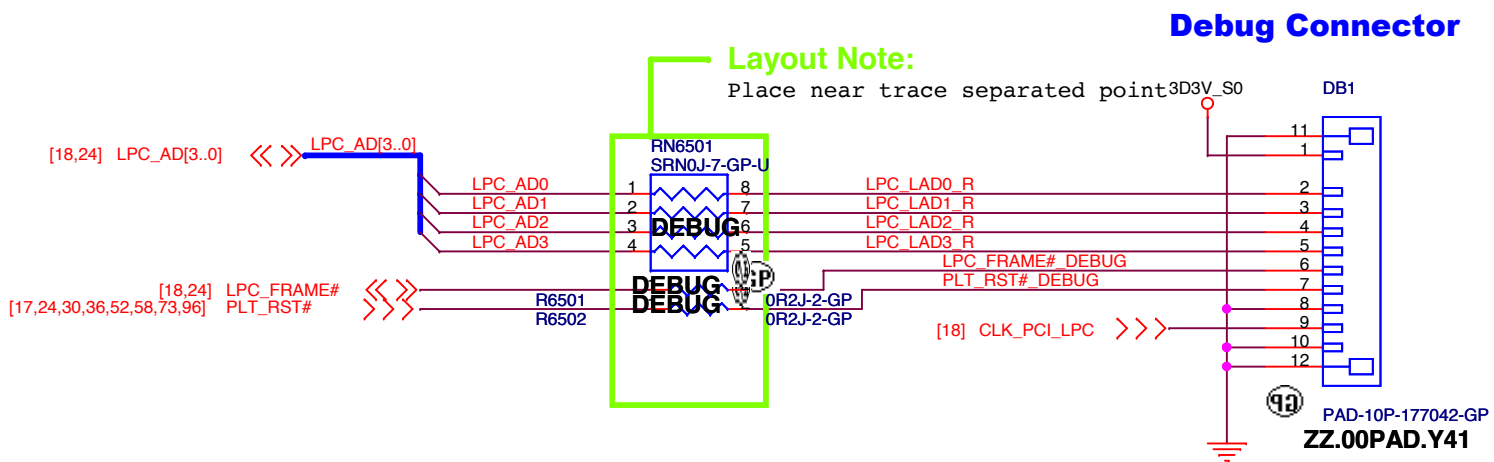


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Title Hall Sensor			
Size A4	Document Number Janus HSW 40/50/70		Rev A00
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SSID = DEBUG PORT



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

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USB3.0 PORT


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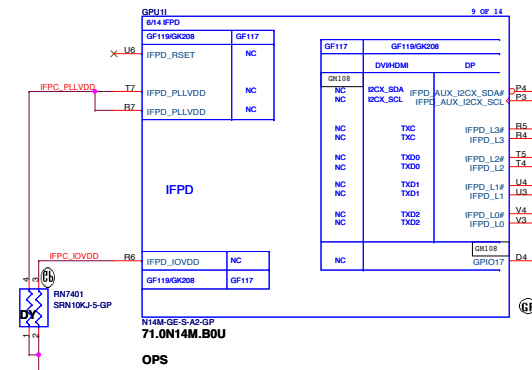
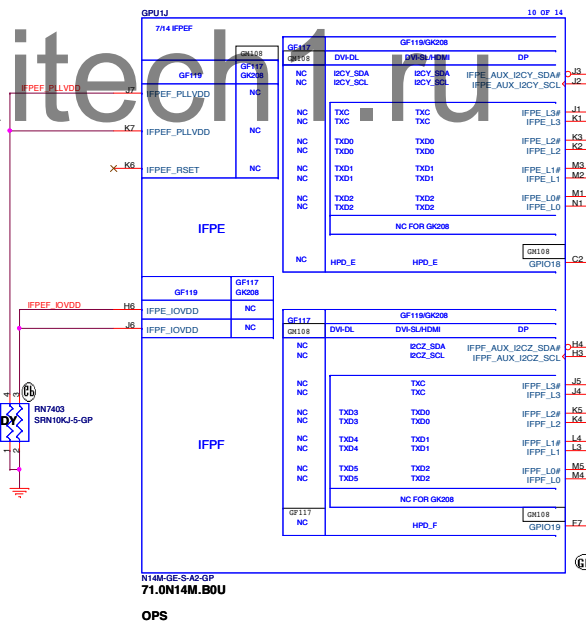
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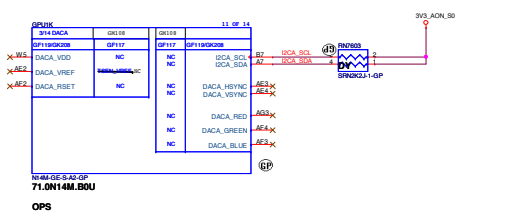
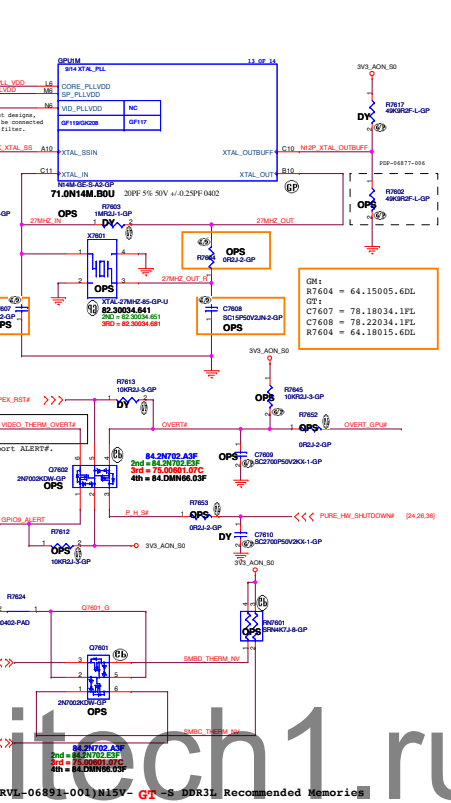
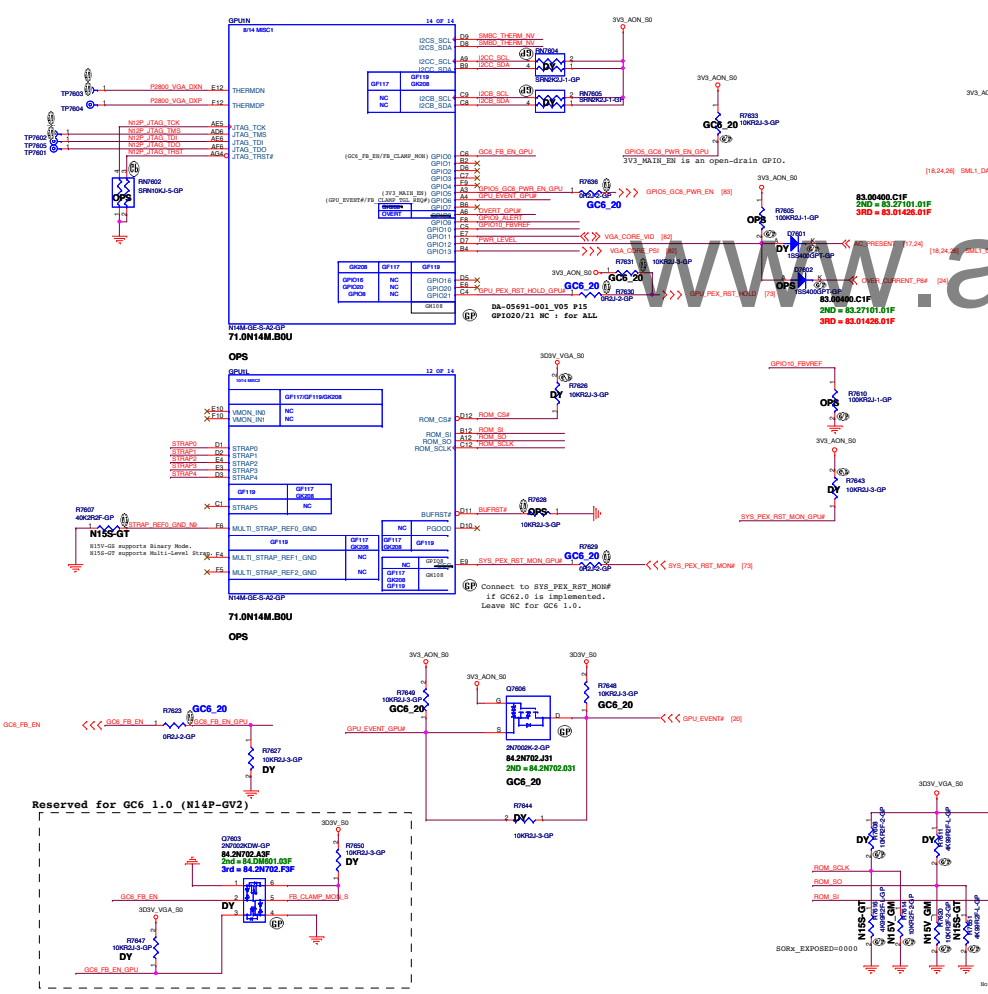


Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVDD	0.1 μ F	X7R	0402	Under GPU
		22 μ F	X5R	0805	Near GPU
		Bead Type			
		30 Ω (ESR=0.05)	0402	1	Near GPU

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Filtering Combined

GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB2B-64	SP_PLLVDD + VID_PLLVDD	0.1 μ F	X7R	0402	Under GPU
GB4B-128		4.7 μ F	X5R	0603	Near GPU
GB3-256		22 μ F	X5R	0805	Near GPU
		Bead Type			
		180 Ω (ESR=0.2)	0603	1	Near GPU



(RVL-06891-001) N15V- GT-S DDR3L Recommended Memories

		Strap		STRAP3	STRAP2	STRAP1	STRAP0
128Mx16 DDR3L	Hynix	Ox9	H5TC2G63FFR-11C	1	1	0	0
	Micron	OxA	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	OxB	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	Ox3	H5TC4G63AFR-11C	0	1	0	0
	Micron	Ox4	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	Ox5	K4W4G1646D-BC1A	1	0	0	1

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 k Ω	1000	0000
10.0 k Ω	1001	0001
15.0 k Ω	1010	0010
20.0 k Ω	1011	0011
24.9 k Ω	1100	0100
30.1 k Ω	1101	0101
34.8 k Ω	1110	0110
45.3 k Ω	1111	0111

Straps

(DS-06814-001)

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VEHODR	10k Ω	+Pull-up to 3V3 if VBIOS ROM exists +Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See note below
STRAP1	RAM_CFG[1]	10k Ω	See note below
STRAP2	RAM_CFG[2]	10k Ω	See note below
STRAP3	RAM_CFG[3]	10k Ω	See note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

(RVL-06891-001) N15V- GM-S DDR3L Recommended Memories

		Strap		STRAP3	STRAP2	STRAP1	STRAP0
128Mx16 DDR3L	Hynix	OxC	H5TC2G63FFR-11C	1	1	0	0
	Micron	Ox1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	Ox5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	Ox4	H5TC4G63AFR-11C	0	1	0	0
	Micron	OxD	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	Ox9	K4W4G1646D-BC1A	1	0	0	1

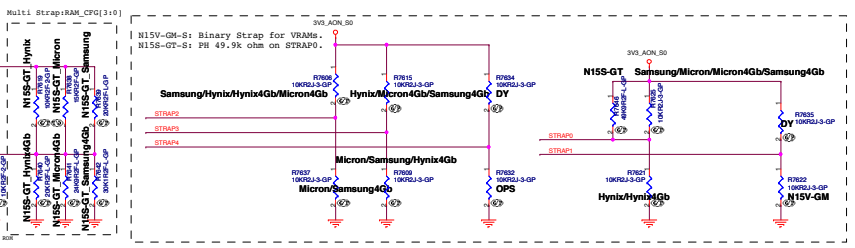
(DS-06814-001)

Table 10. Multi-Level Strap Differences

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	N155-GV	PCI_DEVID[4]	SUB_VEHODR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	N155-GM/-GT	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SO	N155-GV	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	N155-GM/-GT	DEVID_SEL	PCIE_CFG		
STRAP1	N155-GM/-GT	USER[3]	USER[2]	USER[1]	USER[0]
STRAP2	N155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50k pull-up)			
STRAP3	N155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP4	N155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			

DS-06812

Chip	N15V-GM	N155-GT
Device ID	N15V-GM	N155-GT
Memory interface	Q1140	Q1141
Package	595 ball BGA 23x23mm	408 ball BGA 29x29mm





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GPU-VRAM5,6 (3/4)

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GPU-VRAM7,8 (4/4)

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Document Number

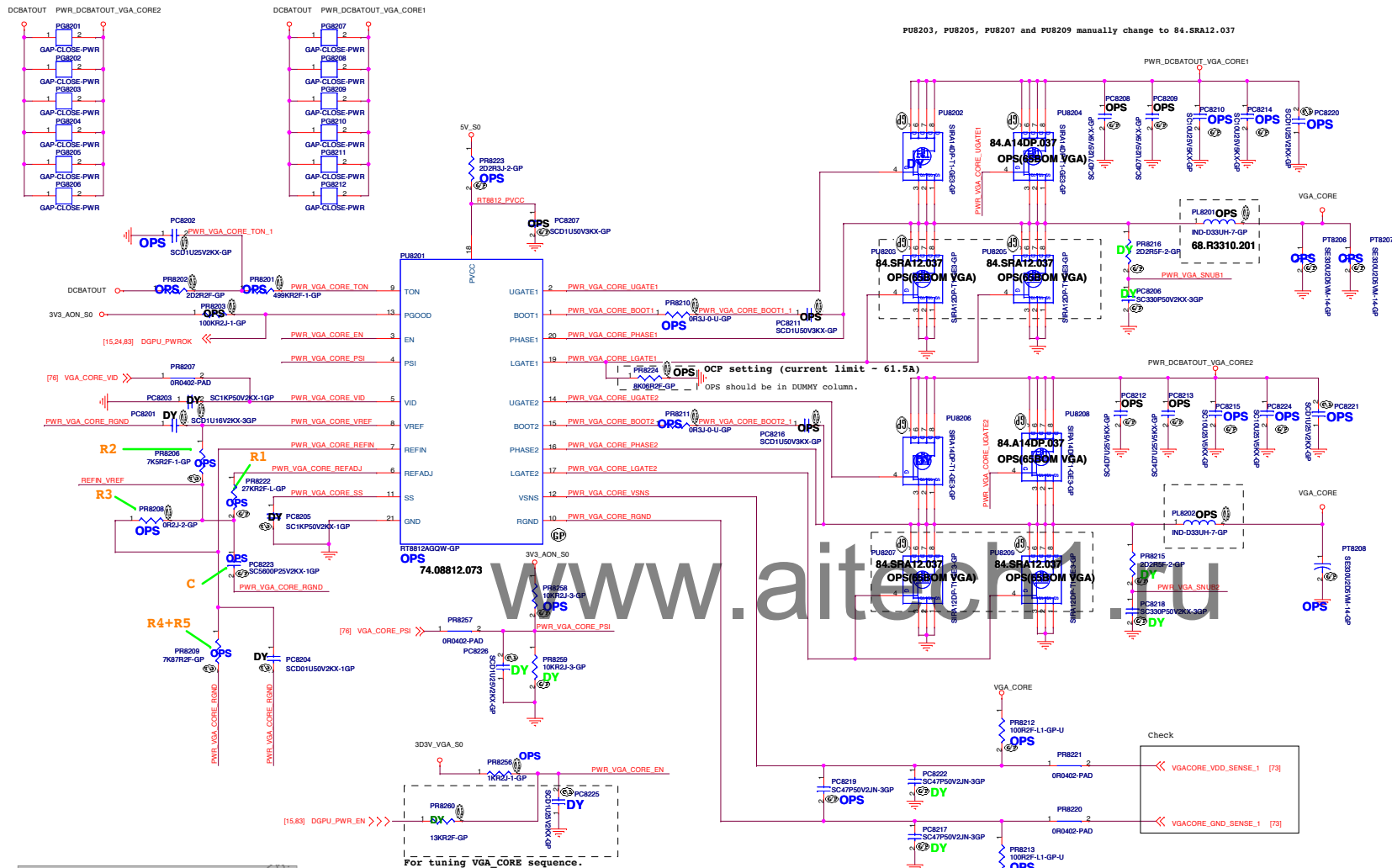
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PUR203, PUR205, PUR207 and PUR209 manually change to 84.SRA12.037

N15V_GM_S Config D

Design Current=33.5A
56.65A <OCP< 66.7A

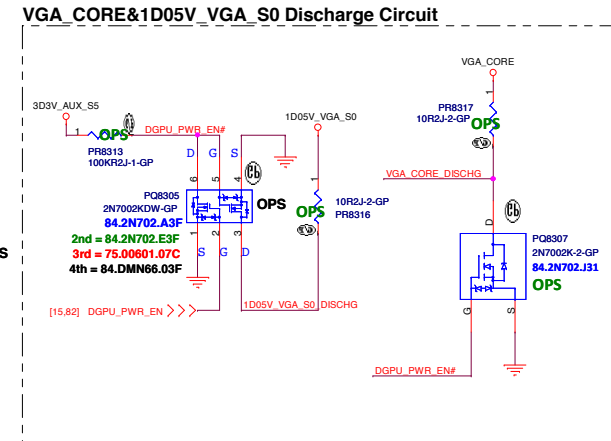
Component	N15V-GM-S Config D	N15-S-07-S Config B
R1 (PR8222)	27K	20K
R2 (PR8204)	64.27025,60L	64.20025,60L
R3 (PR8208)	7.5K	20K
R4+R5 (PR8209)	64.75015,60L	64.20025,60L
C (PC8223)	0	2K
	63.80034,10L	64.20015,60L
	7.87K	18K
	64.78715,60L	64.18025,60L
	5.4nF	2.7nF
	78.56222,2FL	78.27224,2FL

PWM-VID Specification	Config A	Config B	Config C	Config D
Vmin	0.6	0.6	0.6	0.9
Vmax	1.2	1.2	1.15	1.15
Vboot	0.875	0.9	0.9	1.028
Voltage Step Vstep	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	20	20
PWM Frequency F _{min}	1.125	0.676	0.676	
PWM Minimum Pulse Width T _{min}	9.26	74	74	
VID Transient Time T	<100	<100	<100	
Component Value				
R1 (1k)	KQ	39	20	39
R2 (1k)	KQ	39	20	30
R3 (1k)	KQ	1.5	2	3
R4 (1k)	KQ	30	18	24
R5 (1k)	KQ	1.5	0	3
C	nF	1.5	2.7	1.8

I/P cap: 10U 25V X805 X5R/ 78.10622.51L
Inductor:CHIP CHORE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm4.5Vgs/ 84.A14DP.037
L/S: SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm4.5Vgs/ 84.SRA06.037

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3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0
```



CTx (pF)	Rise Time (ns) 10% - 90%, COUT = 0.1µF @ VIN; VOUT=0 ohm load							
	Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562


Table 1. Rise time vs. CTx value

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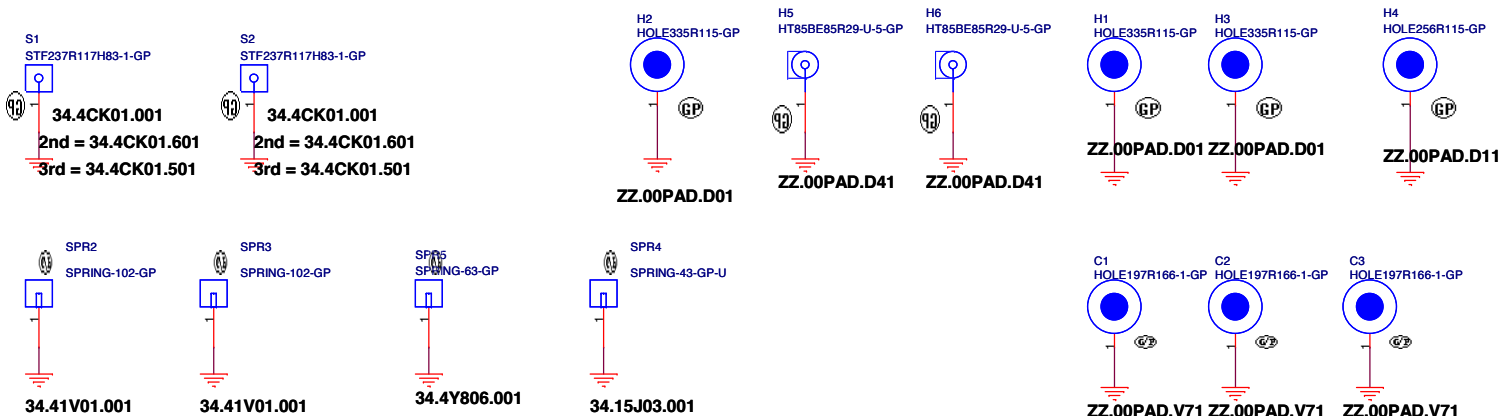
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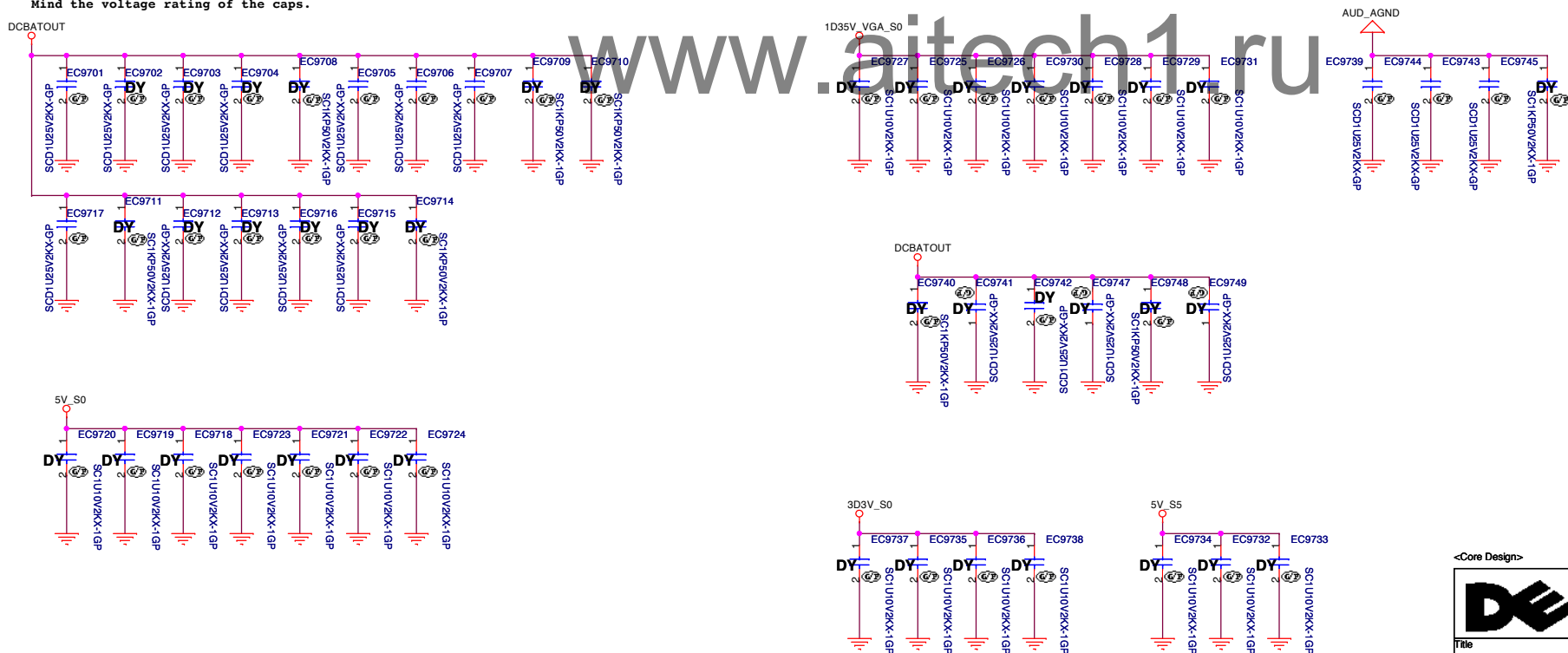
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SSID = Mechanical



SSID = EMI

Mind the voltage rating of the caps.




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Free Fall Sensor


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LVDS Switch

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CRT Switch

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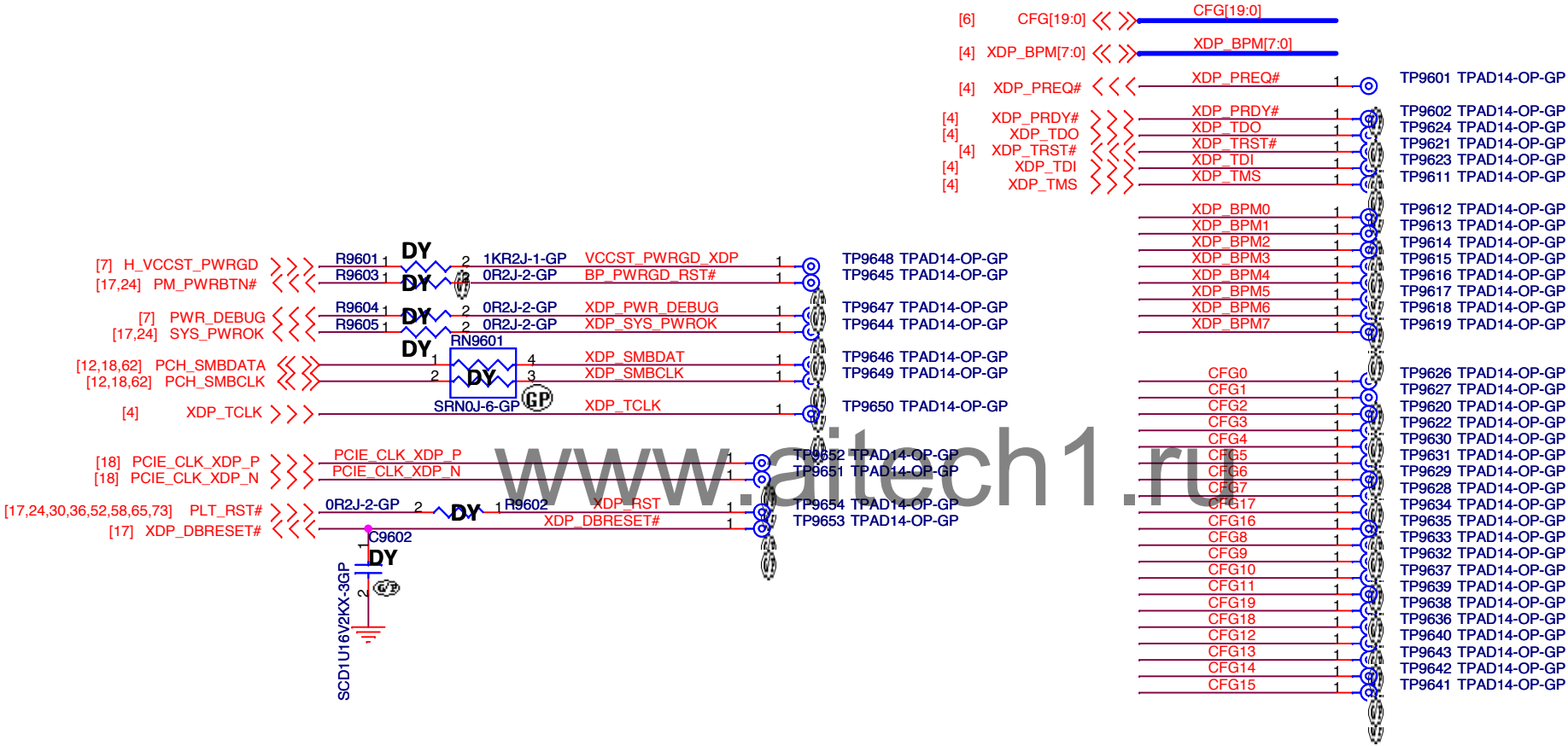
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SSID = XDP

CPU XDP



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CPU/PCH XDP

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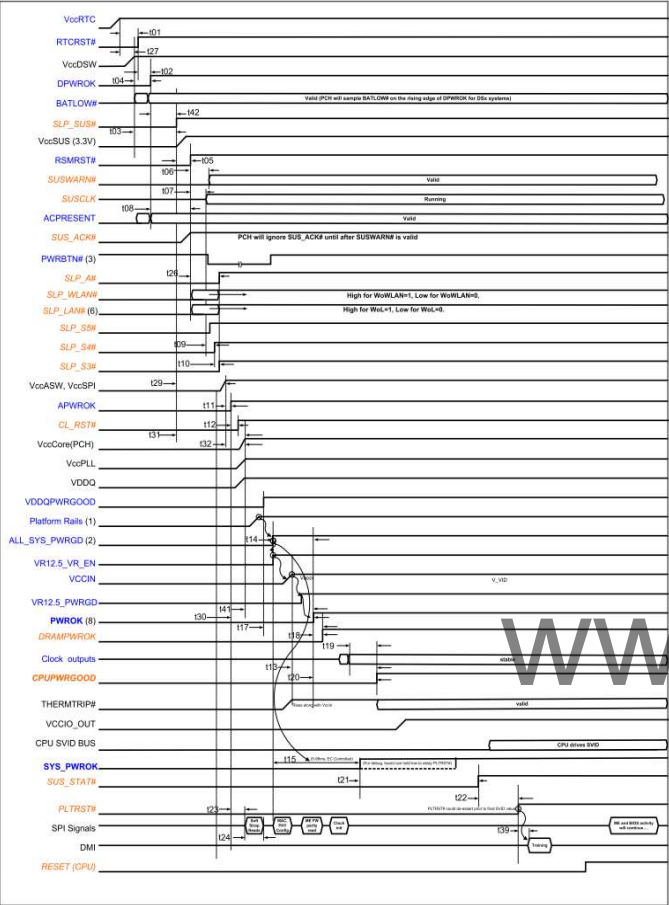
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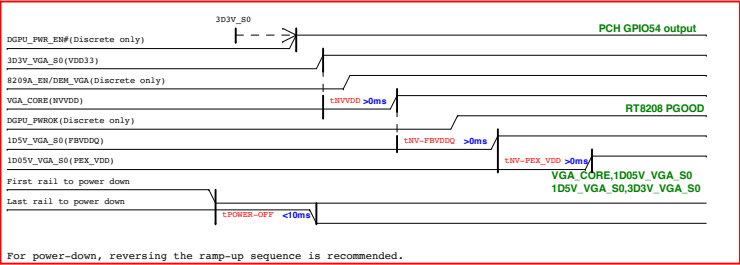
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Shark Bay Platform Power Sequence

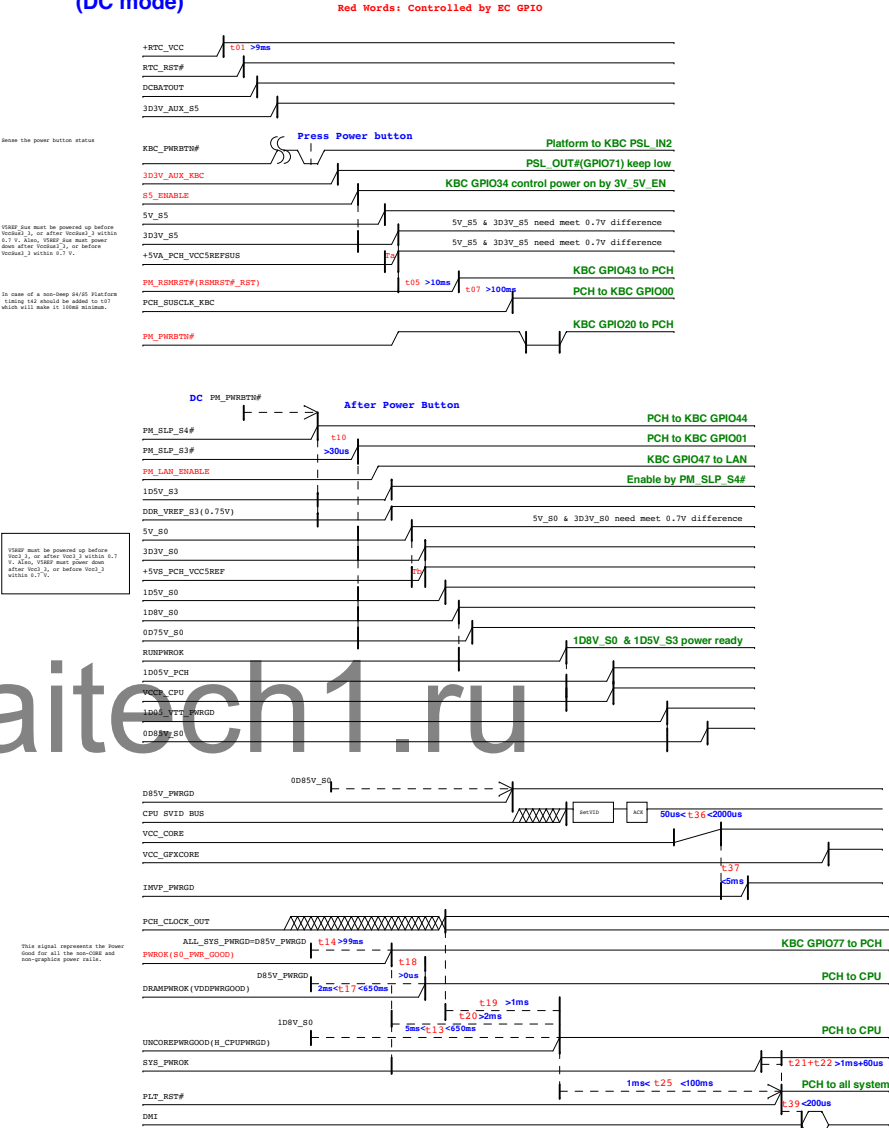


N14P-GT Power-Up/Down Sequence

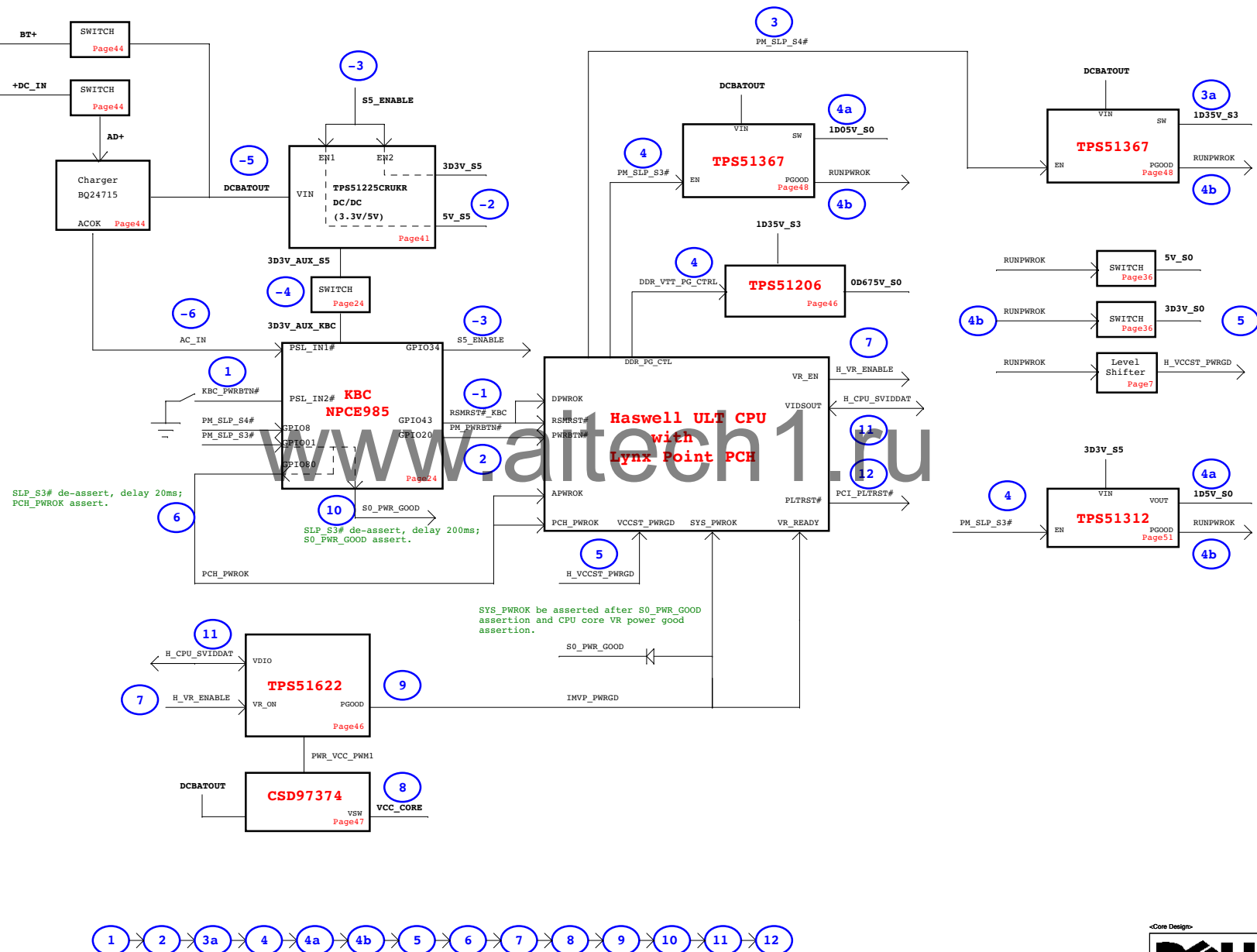


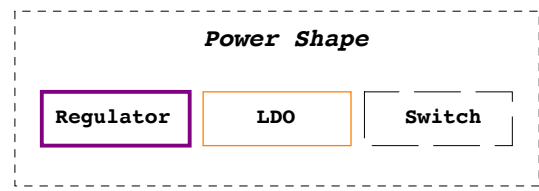
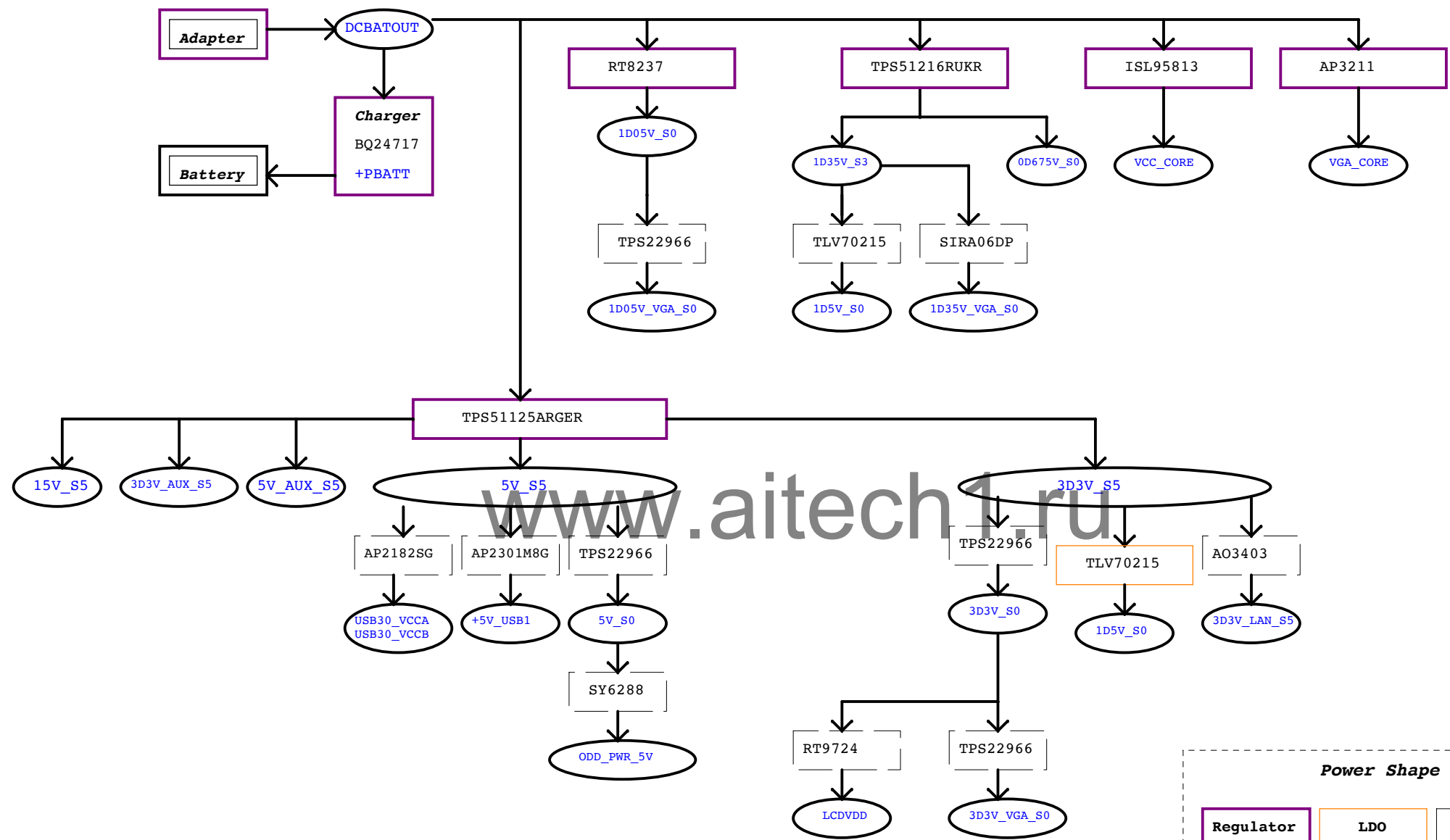
For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

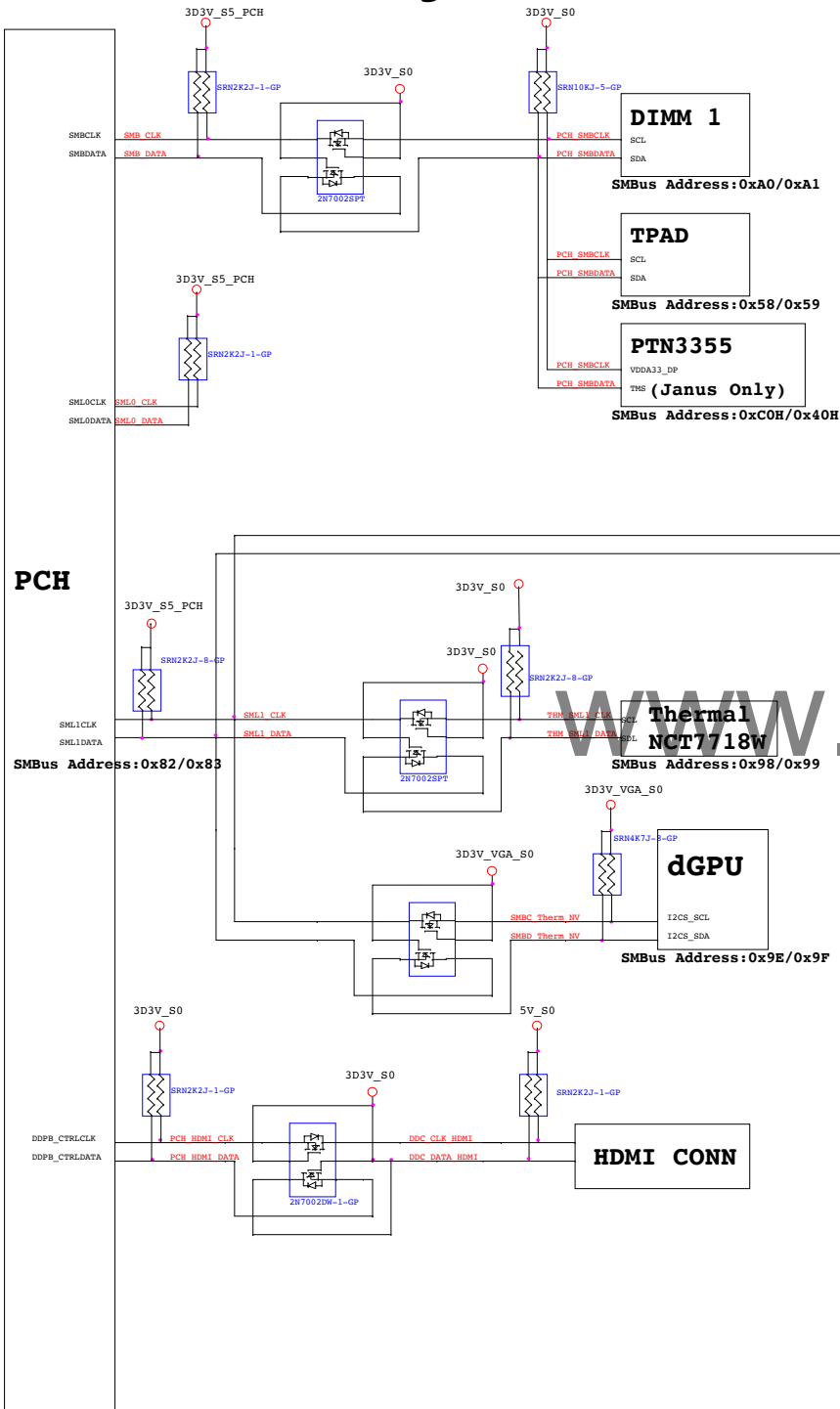


Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM

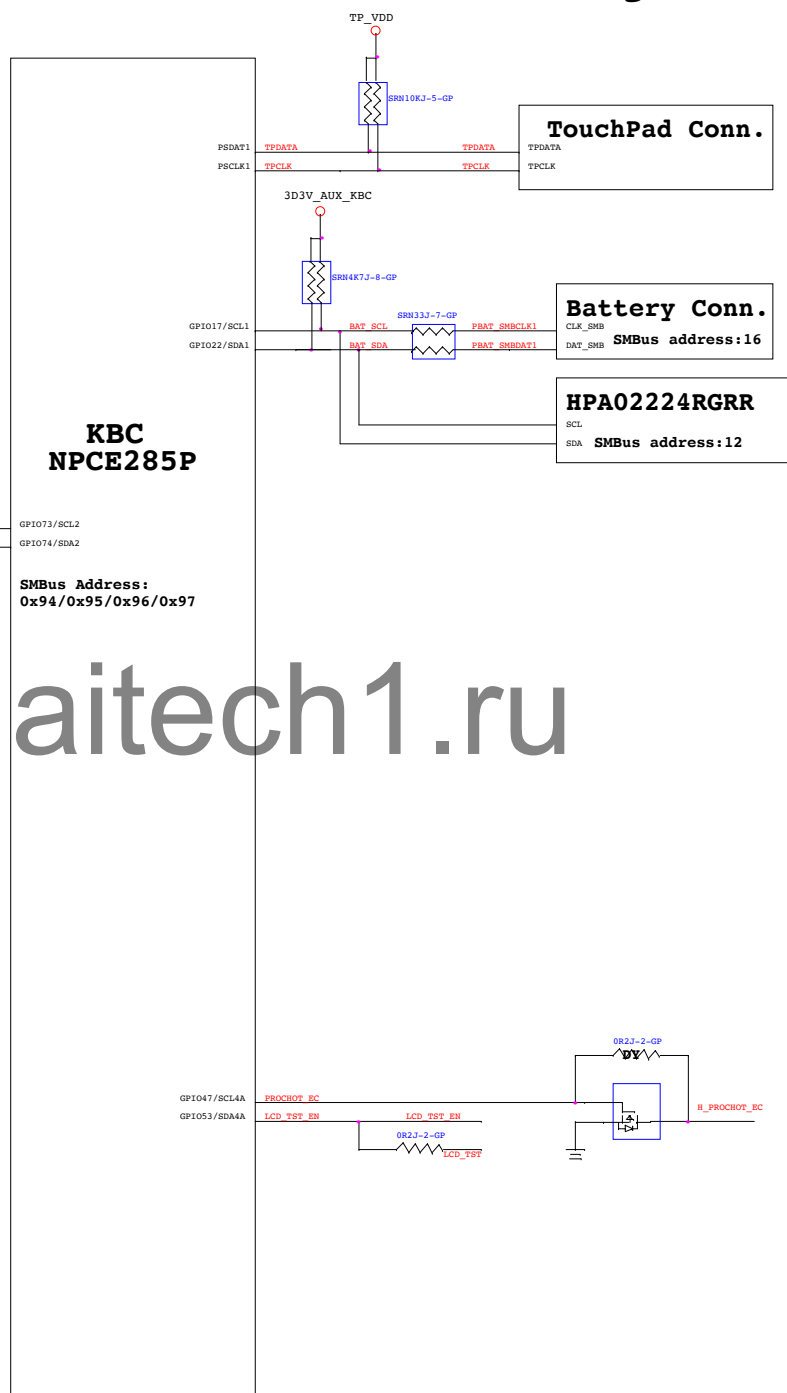




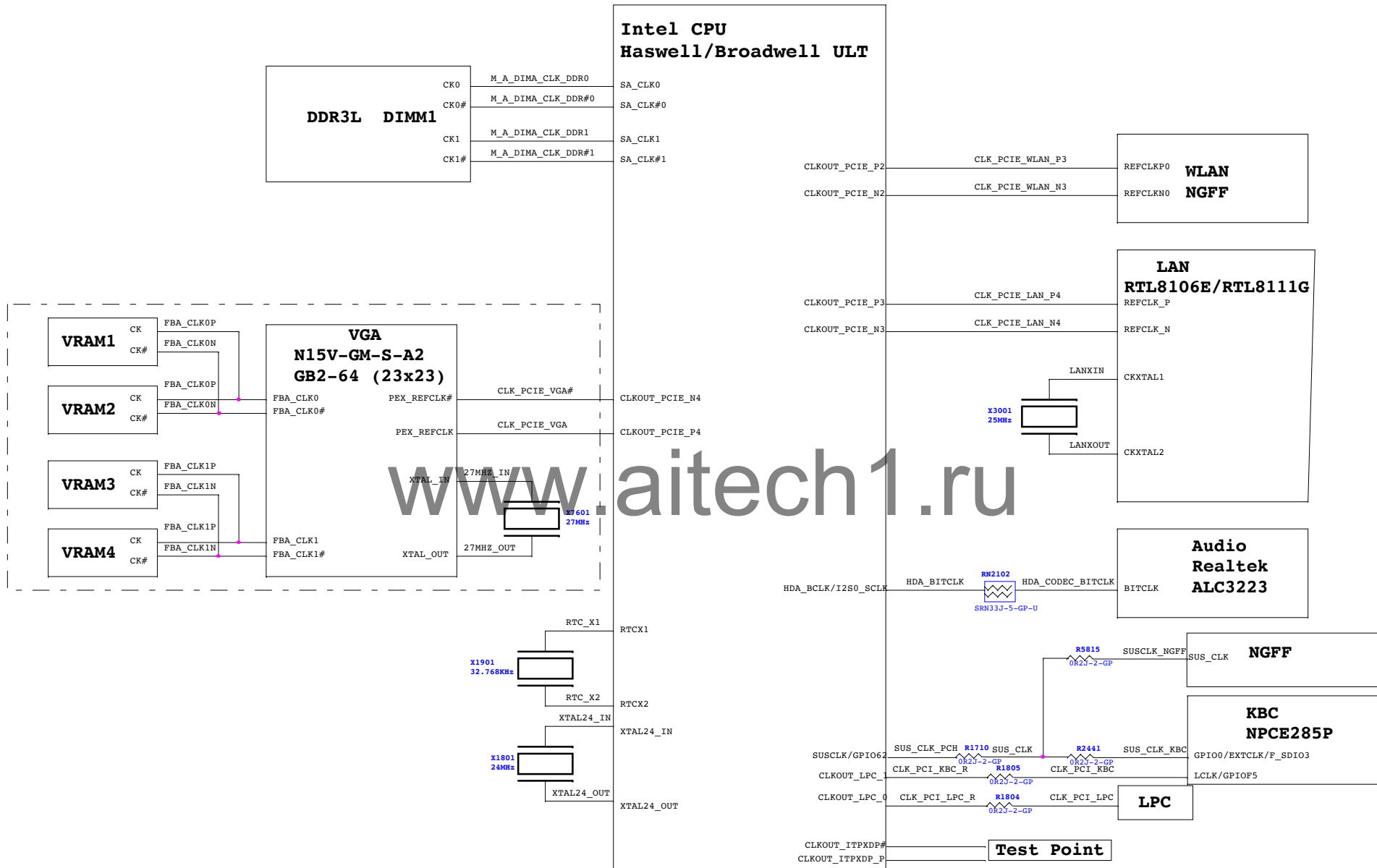
PCH SMBus Block Diagram



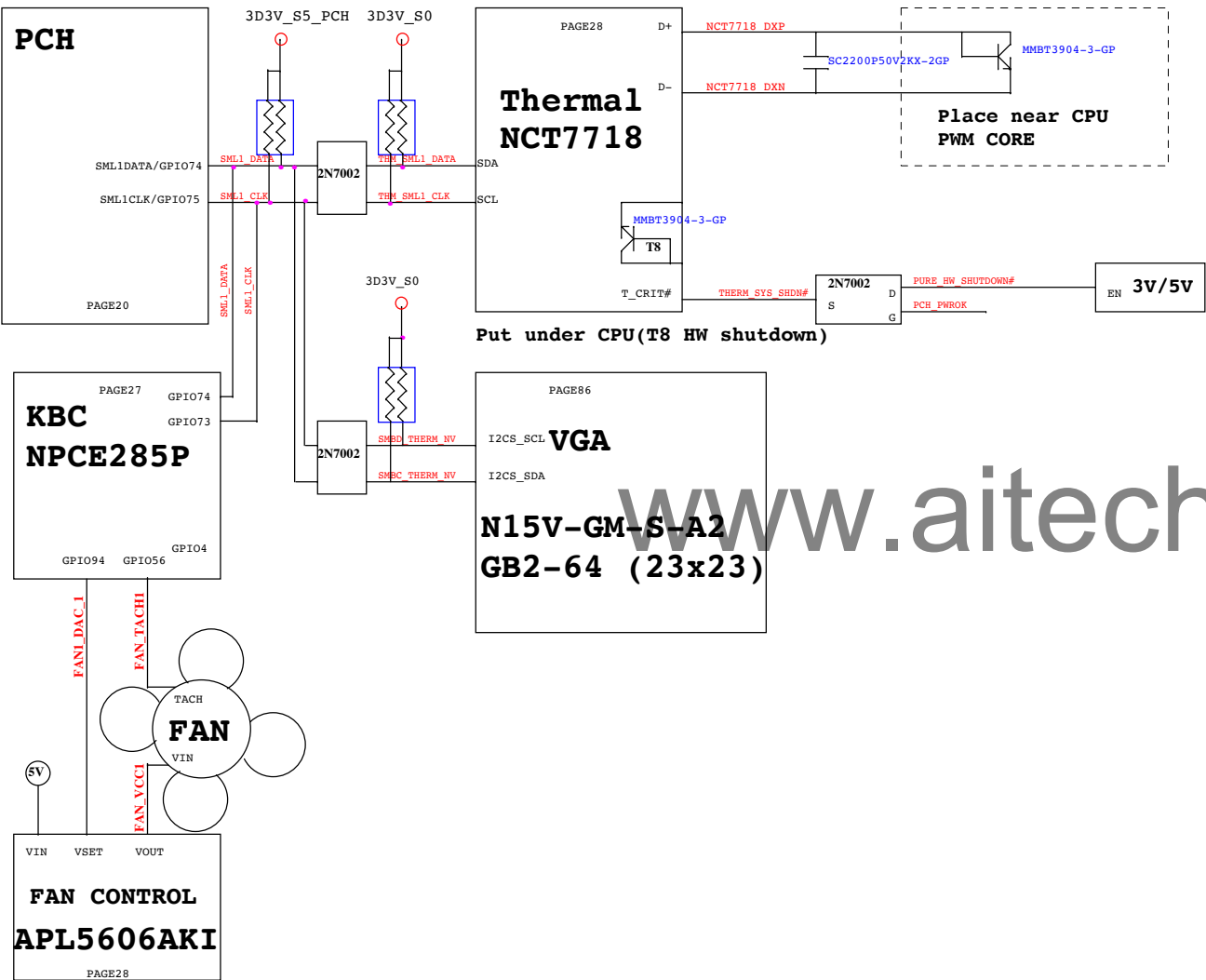
KBC SMBus Block Diagram



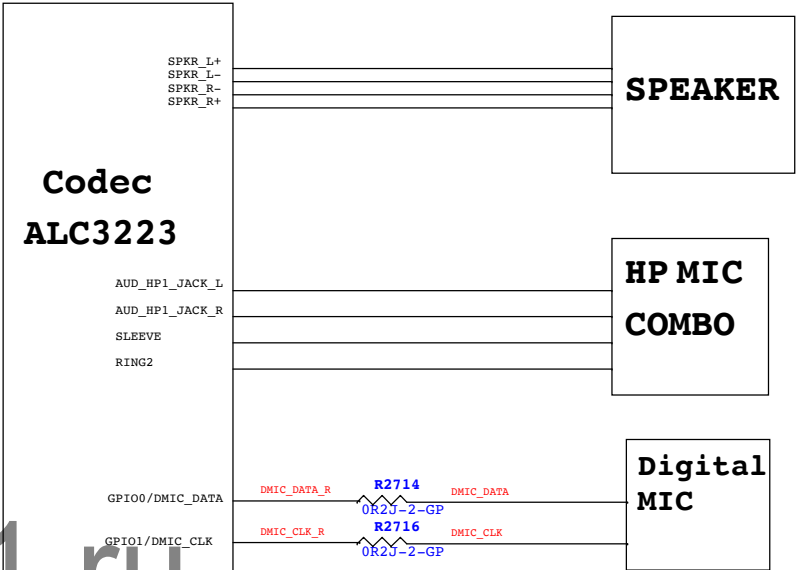
CLK Block Diagram



Thermal Block Diagram



Audio Block Diagram



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